

REMARKS

Claims 1-18 will be pending upon entry of the present amendment. Claims 1-2, 9-11, and 15 are being amended. Claims 16-18 are being newly presented.

Claims 1-5 and 9-15 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,232,642 to Yamazaki. Claims 6-8 were rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki in view of EP patent application 442,413 of Iwazaki.

The claims are not anticipated by or rendered obvious in view of Yamazaki because Yamazaki is not prior art. Yamazaki is based on a U.S. patent application filed June 24, 1998. The claimed invention was conceived and reduced to practice prior to June 24, 1998, as explained in more detail below. Accordingly, claims 1-18 are in condition for allowance.

The present application claims priority from U.S. Patent Application No. 09/442,834, filed on November 18, 1999, issued as U.S. Patent No. 6,387,763, and European Patent Application No. 98830694.0, filed on November 19, 1998. Enclosed is an accurate English translation of the priority EP Application No. 98830694.0. As a result, the claim of priority to the EP Application No. 98830694.0 has been perfected.

Also enclosed is a Rule 131 Declaration of one of the inventors, Federico Pio, stating that the inventors were in possession of the invention prior to June 24, 1998. The discussion in the declaration makes clear that the invention was conceived and reduced to practice well before June 24, 1998. The appendices attached to the Declaration are dated as early as December 1997, and fully support the inventor's statements in the Declaration. As a result, Yamazaki is not prior art and does not anticipate or render obvious any of the claims.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable.
Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Federico Pio et al.

SEED Intellectual Property Law Group PLLC



Robert Iannucci
Registration No. 33,514

RXI:asl

Enclosures:

Postcard

Rule 131 Declaration

Appendices 1-4

English Translation of EP Application No. 98830694.0

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031
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APPENDIX 1

F6X

Process flow (1)

- Lot formation (CZ, high flatness, thickness=675 μ m, resistivity= 08-12 Ohm/cm)
- Denuding (180 Å, 1100°C, N₂/O₂)



Alignment marks mask (105)

- oxide and silicon etch
- resist removal
- Denuding oxide removal (200Å, HF 1:20)
- RECESSED LOCOS stack formation
 - ✓ pad oxide growth (100 Å, 800°C, H₂/O₂ + DCE)
 - ✓ nitride deposition (1170 Å, 775°C ramped, 300 mT)



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Process flow (2)



Active area mask (105)

- nitride and oxide etch
- silicon dry etch (500Å) (trials for 1000Å trench depth)
- resist removal

- Field oxide growth (5700 Å, 1000°C, H₂/O₂) (trials for 5500Å, 1100°C)
- Oxinitride removal
- Nitride removal

- Oxide removal
- Sacrificial oxidation (400 Å, 875°C, H₂/O₂ + DCE)

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Process flow (3)

Capacitor implant mask (265)

- UV cure
 - ✓ capacitor implant (P31, 5.0E14 cm-2, 80 KeV, tilt=8 Deg)
- resist removal
- Field oxide recover and capacitor implant annealing (950°C, N2, 60')

N-well mask (015)

- ✓ n-well implant (P31, 1.0E13 cm-2, 1.2 MeV, tilt=8 Deg, twist=55 Deg)
- ✓ HV&LV n-iso implant (P31, 3.0E12 cm-2, 500 KeV, tilt=8 Deg)
- ✓ p-ch HV&LV LVS implant (B11, 1.7E12 cm-2, 25 KeV, tilt=7Deg)
- ✓ p-ch HV&LV aPT implant (P31, 1.0E12 cm-2, 180 KeV, tilt=7 Deg)
- resist removal

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Process flow (4)

P-iso mask (255)

- ✓ HV&LV p-iso implant (B11, 3.5E12 cm-2, 180 KeV, tilt=8 Deg)
- resist removal

P-well mask (055)

- ✓ p-well implant (B11, 1.0E13 cm-2, 700 KeV, tilt=8 Deg, twist=55 Deg)
- ✓ n-ch HV&LV LVS implant (B11, 1.5E12 cm-2, 50 keV, tilt=7 Deg)
- resist removal

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Process flow (5)

n-ch LVS mask (355)

- n-ch LV LVS implant (B11, 4.2E12 cm-2, 50 KeV, tilt=7 Deg)
- n-ch LV aPT implant (B11, 4.0E12 cm-2, 140 KeV, tilt=7 Deg)
- resist removal

p-ch LVS mask (375)

- p-ch LV LVS implant (B11, 2.0E12 cm-2, 25 KeV, tilt=7 Deg)
- p-ch LV aPT implant (P31, 2.0E12 cm-2, 180 KeV, tilt=7 Deg)
- resist removal

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Process flow (6)

- Sacrificial oxide removal (550 Å, HF 1:20)
- HV oxide growth (150 Å, 800°C, H₂/O₂ + DCE)

HV mask (455)

- HV oxide removal (diluted BOE, 270Å)
- resist removal
- LV oxide growth (100 Å, 750°C, H₂/O₂)

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Process flow (7)

Tunnel area mask (405)

- UV cure
- descumming
- oxide removal (diluted BOE, 140Å for DP FLOTOX, 350Å for SP FLOTOX)
- resist removal

- Tunnel oxide growth (60 Å, 900°C, N₂/O₂ + DCE, N₂ 1000°C)

- Poly1 deposition:

- ✓ (1000 Å, 530°C, 280 mT, in situ doping P 7.0E19 cm⁻³) for DP FLOTOX
- ✓ (3500 Å, 530 °C, 280 mTorr, in situ doping P 25E19 cm⁻³) for SP FLOTOX

EPM mask (275) for DP FLOTOX, ONLY

- cell aPT implant (B11, 1.0E12 cm⁻², 240 KeV, tilt=7 Deg , twist=55 Deg)
- resist removal

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Process flow (8)

SP FLOTOX and DP FLOTOX



Poly mask (505)

- polysilicon dry etch
- resist removal



FG mask (556)

- poly1 dry etch
- resist removal
- ONO formation
 - ✓ bottom oxide growth (50 Å on mono/85 Å on poly, 900°C, O₂/N₂)
 - ✓ nitride and HTO top oxide depositions (80 Å nitride + 85 Å oxide)

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Process flow (8a)

DP FLOTOX

- Dummy poly deposition (500Å, 530°C, 280 mT, in situ doping P 2.0E20 cm-3)

Matrix mask (525)

- dummy poly dry etch
- ONO dry etch
- resist removal

- Poly2 deposition (1000 Å, 530°C, 280 mT, in situ doping P 2.5E20 cm-3)
- WSi2 deposition (1500 Å)

Poly mask (505)

- WSi2 and poly dry etch
- resist removal

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Process flow (8b)

DP FLOTOX



Self aligned mask (515), DR

- ONO dry etch
- poly1 dry etch
- resist removal

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Process flow (9)

- 1st S&D reoxidation (170 Å, 900°C, O₂)

N- implant mask (615)

- n- implant (P31, 4x(5.0E12) cm⁻², 70 KeV, tilt=45 Deg)
- resist removal

P- implant mask (645)

- p- implant (BF₂, 1.0E13 cm⁻², 100 KeV, tilt=0 Deg)
- resist removal

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Process flow (10)

- TEOS deposition (4000 Å, 700°C ramped, 250 mT)
- spacers dry etch
- descumming

N+ implant mask (605)

- UV cure
- n0 implant (P31, 4x(5.0E13) cm-2, 80 KeV, tilt=45 Deg)
- n+ implant (As, 4.0E15 cm-2, 35 KeV, tilt=0 Deg)
- resist removal

- 2nd S&D reoxidation (100Å, 900°C, O2) for SP FLOTOX, (trials for DP FLOTOX)

P+ implant mask (655)

- p+ implant (BF2, 3.0E15 cm-2, 40 KeV, tilt=0 Deg)
- resist removal

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Process flow (11)

- Backside removal
- descumming
- interlevel dielectric deposition (to be fixed for SP FLOTOX)
 - ✓ TEOS deposition (1000 Å, 700°C ramped, 250 mT)
 - ✓ BPSG 2:9 deposition (14500 Å)
 - ✓ BPSG densification (RTP, 1050°C, N₂, 30 sec)
- CMP interlevel dielectric etch (to be fixed for SP FLOTOX)

Contact mask (705)

- contact dry etch
- resist removal

N+ contact implant mask (735)

- n+ contact implant (As, 1.0E15 cm⁻², 60 KeV, tilt=0 Deg)
- resist removal

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Process flow (12)



P+ contact implant mask (645)

- p+ contact implant (BF₂, 6.0E14 cm⁻², 20 KeV, tilt=0 Deg)
- resist removal

- Contact implant activation (RPT, 810°C, N₂, 30 sec)

- Contact cleaning (FPN 30 sec)

- First barrier deposition (collimated Ti 350 Å + TiN 1000 Å)

- barrier stuffing (RTP, 750°C, N₂, 60 sec)

- W deposition (8000 Å)

- W etch-back

- Hot metal1 deposition (Ti 100Å + Al/Cu 4000 Å + TiN 350 Å, 480°C)



Metal1 mask (800)

- metal1 etch

- resist removal

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Process flow (13)

- First intermetal dielectric deposition (to be fixed for SP FLOTOX)
 - ✓ HDPCVD USG deposition (6000 Å)
 - ✓ TEOS deposition (12000 Å)
- CMP intermetal dielectric etch (to be fixed for SP FLOTOX)



Vias 1 mask (850)

- vias dry etch
- resist removal
- Second barrier deposition (Ti 500 Å + TiN 1000 Å)
- W deposition (8000 Å)
- W etch-back
- Hot metal2 dep. (Ti 100Å + Al/Cu 5500 Å + TiN 350 Å, 480°C)

F6X

Process flow (14)

Metal2 mask (860)

- metal2 dry etch
- resist removal

● Second intermetal dielectric deposition (to be fixed for SP FLOTOX)

- ✓ HDPCVD USG deposition (6000 Å)
- ✓ TEOS deposition (12000 Å)

● CMP intermetal dielectric etch (to be fixed for SP FLOTOX)

Vias 2 mask (870)

- vias dry etch
- resist removal

F6X

Process flow (15)

- Third barrier deposition (Ti 500 Å + TiN 1000 Å)
- W deposition (8000 Å)
- W etch-back
- Hot metal3 deposition (Ti 100Å + Al/Cu 8000 Å + TiN 350 Å, 480°C)



Metal3 mask (880)

- metal3 dry etch
- resist removal
- Al sintering
- Final passivation (oxynitride 4000Å + SOG 4250Å + oxynitride 12000Å + TEOSPSG 4000Å)

F6X

Process flow (16)

Pads mask (900)

- UV cure
- pads dry etch
- resist removal
- Al sintering
- UV erasing and parametric testing

APPENDIX ' 2

SGS-THOMSON MicroelectronicsCONFIDENTIAL

I.C. 127.1047.98

Agrate, 5th May 1998From: P.Zuliani
J.L.OgierTo: F.Riva
A.Saini
A.Sala
T.Borowczak (Rousset)
B.Bos (Rousset)
C.Cremonesi
G.Dalla Libera
N.Galbiati
E.Gomiero
A.Marmioli
J.M.Mirabel (Rousset)
M.Patelmo
F.Pio
O.Pizzuto (Rousset)
M.T.Sala
M.Tormen
B.Vajana
G.Valentini
N.ZatelliF.I.: L.Baldi
G.Crisenza
C.Lombardi

ZZ33 Test Pattern Description

Release 2

Authorized by: L.Baldi

Part 1)

This document is an updated description of the test structures present on the ZZ33 Test Pattern. A partial modification of this mask set has been performed. The following mask levels have been revised:

	<i>Release</i>
mask 105 (active area)	B
mask 265 (capa implant)	B
mask 015 (N-well)	B
mask 055 (no-tub)	B
mask 355 (LVS n-ch)	B
mask 375 (LVS p-ch)	B
mask 385 (LV p-ch Nat)	B
mask 455 (HV oxide)	B
mask 405 (tunnel oxide)	C
mask 556 (Poly1)	B
mask 505 (Poly2)	B
mask 605 (n+ S&D)	B
mask 655 (p+ S&D)	B
mask 705 (contacts)	B
mask 800 (Metal1)	C

The data base corresponding to this partial mask set modification has been loaded in the area: *opustrd/TP-PROC/ zz33a_r3* (the top cell is named ZZ33ATOP; ZZ33A is startfile1 and ZZ33ST startfile2).

ZZ33 is a Test Pattern devoted to the electrical characterization of the devices in CMOS6X technology; it contains the following structures (see fig.1):

- TEGs for transistor characterization NZ_ZZ33_TRANS
- TEGs for field transistor characterization ESSA11
- TEGs for diode and capacitor characterization ZZ33DAZZ12
- TEGs for oxide monitor and characterization TEGOX
- NZ_OXZZ19UPDOWN
- TEGs for EEPROM SP cell characterization NZ_ZZ33_SPTEGSTD
- NZ_ZZ33_SPM
- TEGs for EEPROM DP cell characterization DLG_VJ_F6XDPCELL
- TEGs for Zener diode characterization RB_ZENER
- spreading resistance test structures RB_SR
- TEGs for ESD characterization ESD_ZZ33_TOP

The following modules will be described in the next pages:

NZ_ZZ33_TRANS

- TEG1, 2: P-ch LV nat and LVS transistors	page 8, 9
- TEG3, 4: P-ch HV Full Drex nat and LVS transistors	page 10,11
- TEG5, 9: N-ch HV nat and LVS transistors	page 12, 16
- TEG6, 10: N-ch HV no-tub nat and LVS transistors	page 13, 17
- TEG7, 11: N-ch HV Full Drex nat and LVS transistors	page 14, 18
- TEG8, 12: N-ch HV no-tub Full Drex nat and LVS transistors	page 15, 19
- TEG13, 14, 16: N-ch LV nat and LVS transistors	page 20, 21, 23
- TEG15: N-ch LV no-tub nat and LVS transistors	page 22
- TEG17, 18: N-ch HV Drex nat and LVS transistors	page 24, 25
- TEG19, 20: N-ch HV no-tub Drex nat and LVS transistors	page 26, 27
- TEG21, 22, 23: P-ch HV Full Drex nat and LVS transistors	page 28, 29, 20
- TEG24: P-ch HV Drex nat and LVS transistors	page 31

RB_ZENER

- TEGs for Zener diodes	page 32, 33
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RB_SR

- Spreading Resistance structures	page 34, 35
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NZ_ZZ33_SPTEGSTD

- TEG SP01: 28 μ m ² Single Poly Cells	page 36
- TEG SP02: 28 μ m ² Single Poly Equivalent Transistor	page 37
- TEG SP03: 28 μ m ² Single Poly Cells without select	page 40
- TEG SP05: 28 μ m ² Single Poly Cells with different tunnel area	page 38
- TEG SP06: 28 μ m ² Single Poly Cells: Sensing and Select transistors	page 39
- TEG SP11: 28 μ m ² Single Poly Cells: Select Transistor in dummy array	page 41
- TEG SP13: HV and LV LVS transistors with different contact-gate distance d	page 49

NZ_ZZ33_SPM

- TEG SP07: Matrix of 28 μ m ² Single Poly Cells	page 42
- TEG SP08: Matrix of 22 μ m ² Single Poly Cells	page 43
- TEG SP09: Matrix of 19 μ m ² Single Poly Cells	page 44
- TEG SP14: ROM Matrix	page 45
- TEG SP10: Matrix of 20 μ m ² Single Poly Cells	page 46
- TEG SP04: Cast of 28 μ m ² , 22 μ m ² , 20 μ m ² , 19 μ m ² Single Poly Cells	page 47
- TEG SP12: Cast Equivalent Transistors of 28 μ m ² , 22 μ m ² , 20 μ m ² , 19 μ m ² Single Poly Cells	page 48

DLG_VJ_F6XDPCELL

- DLGCELL1: F6DP cell, F6X smallest cell, F6X cell	page 50
- DLGCELL2: F6X standard cell (32% shrink)	page 51
- DLGCELTEQ2: Equivalent Transistor of the cells in the teg DLGCELL2	page 52
- DLGCELL3: Dimension variations of F6X standard cell	page 53
- DLGCELTEQ3: Equivalent Transistor of the cells in the teg DLGCELL3	page 54
- DLGCELL4: Small F6X cell	page 55
- DLGCELLTEQ4: Equivalent Transistor of the cells in the teg DLGCELL4	page 56
- DLGCELL5: Advanced F6X cell (36% shrink)	page 57
- DLGCELLTEQ5: Equivalent Transistor of the cells in the teg DLGCELL5	page 58
- DLGCELL6: F6X Byte and Small F6X Byte	page 59

- DLGCELL7: Advanced F6X Byte and Advanced F6X Bytone	page 60
- DLGCELL8: Bytone and Small F6X Bytone	page 61
- DLGCELL9: F6X Cast (512K), Advanced F6X Cast (512K), Small F6X Cast (512K) and noDPCC F6X Cast (512K)	page 62
- DLGCELL10: Advanced F6X cell (36% shrink) with capa implant on the source line	page 63
- DLGCELLTEQ10: Equivalent Transistor of the cells in the teg DLGCELL10	page 64
- DLGCELL11: Advanced F6X cell (36% shrink): dimension variations	page 65
- DLGCELLTEQ11: Equivalent Transistor of the cells in the teg DLGCELL11	page 66
- DLGCELL12: F6X Miscellanea	page 67
- DLGCELL13: No self-aligned F6X Cell	page 68
- DLGSELECT: Select Transistors in dummy array	page 69

The description of module ESD_ZZ33_TOP is in the I.C.138.1047.97 by P.Colombo.

The description of modules TEGOX and NZ_OXZZ19UPDOWN are in the I.C. by C. Clementi.

The description of the module ZZ33DAZZ12 is in the ZZ12 T.P. description (P.Ghezzi, A.Grossi, I.C.115.1047.96), at pages C44-C52.

The following TEGs have been modified:

1) Transistors

- **TEG2** for p-ch LV nat and LVS transistors with minimum width $W=0.45\mu\text{m}$
- **TEG9** for n-ch HV nat full drex transistors with minimum width $W=0.45\mu\text{m}$ and varying contact to gate distance
- **TEG10** for n-ch HV nat no-tub full drex transistors with minimum width $W=0.45\mu\text{m}$ and varying contact to gate distance
- **TEG16** for n-ch LV nat and LVS transistors with minimum width $W=0.45\mu\text{m}$
- **TEG21** for p-ch HV nat and LVS full drex transistors with p+ ring around contacts (p+ enclosure of contacts = 0.0)
- **TEG22** for p-ch HV nat and LVS full drex transistors with p+ ring around contacts and varying p+ ring dimensions (typical: p+ to gate distance= $1.0\mu\text{m}$, active area enclosure of p+ = $0.6\mu\text{m}$, p+ enclosure of contacts= 0.0)
- **TEG23** for p-ch HV nat and LVS full drex transistors with minimum width $W=0.45\mu\text{m}$.

2) Zener

- **TEG ZENER:** for structures corresponding to pads 1-9, the poly has been aligned to capa implant
- **TEG ZENER2:** for structures corresponding to pads 1-13, the poly has been aligned to capa implant

3) Single Poly Cells

- The layout has been modified to obtain the p-well implant, the "natural" layer, the HV oxide on the sensing transistor of the cell (previously the cells were realized in no-tub LVS regions and sensing transistor was LV).
- TEGs SP05, SP08, SP09: some byte switch transistor is a "no-tub" one

4) ROM matrix

- TEG SP14: the drain extension layer has been drawn to half gate (formerly it was aligned to source line including all gate

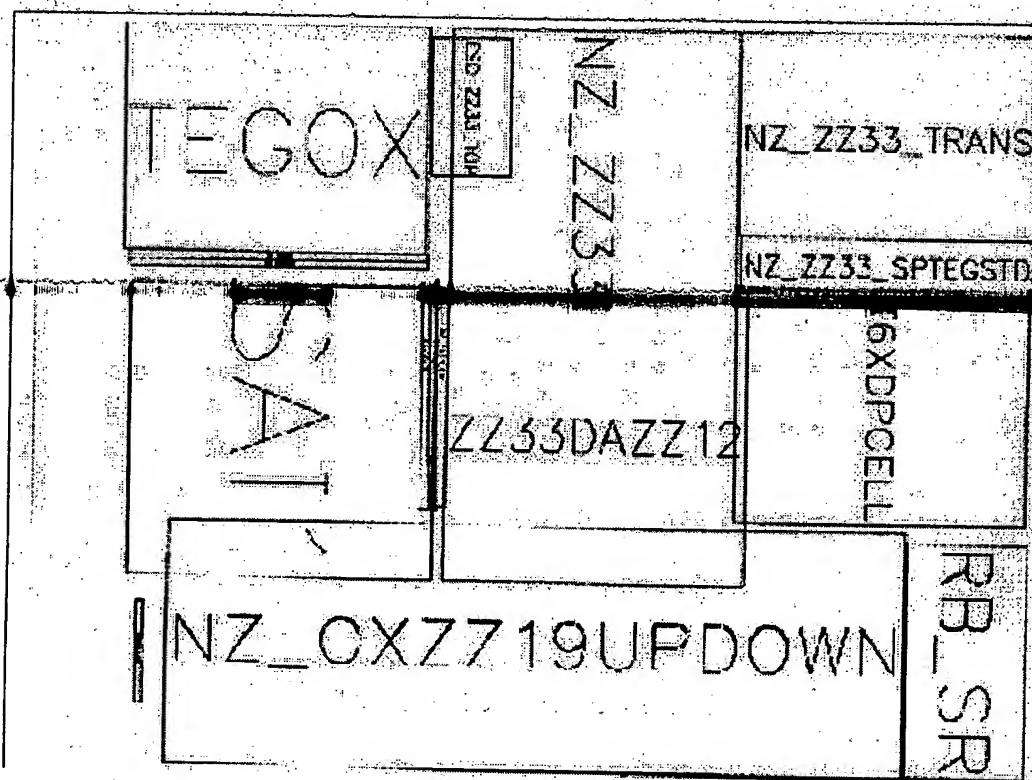
5) Double Poly Cells

- The layout of the Double Poly cells has been modified, according to the results from lots out processed with the existing masks set. The cell is realized in the p-well (no-tub layer has been eliminated from the array); it is natural (no N-ch LVS implants) and HV. The tunnel window is a stripe (the mask extends both on field oxide and on active between select transistor and floating gate transistor). The active "T" shape has been modified so that Select Transistor width is larger than memory transistor width. Poly1 is not crossing source line. Several geometrical variations have been included and the CASTs have also been accordingly modified.

The merging flow is *cmof6xtp_FULL.kaz* (April, 14th, 1998)

MASK	Field	Mask Name	Merging Program	O.V./side
015	D	N-well	1	
055	C	No-tub	[(2 AND 3) OV +0.6] OR 1	
105	C	Active Area	2	0.25
255	C	P-iso	-Not used-	
265	D	Capa Implant	40	
275	D	EPM/ ROM code	48	
355	C	LVS n-ch	56 OR 1	
375	D	LVS p-ch	1 MINUS (58 AND 56)	
385	D	P-ch nat	1 MINUS 56	
405	D	Tunnel	59	-0.05
455	C	HV oxide	58	
505	C	Poly	13	
515	D	Self Aligned	37	
525	C	Matrix	54	
556	D	Floating Gate	35	
605	C	N+ diffusion	17 OR 57	
645	D	P- diffusion	17	
655	D	P+ diffusion	17 MINUS 57	
705	D	Contacts	19	-0.05
735	C	N+ contacts	2 AND 17	
745	D	P+ contacts	2 AND 17	
800	C	Metal1	23	
850	D	Vias1	25	
860	C	Metal2	27	
870	D	Vias2	32	
880	C	Metal3	34	
900	D	Passivation	30	

TEST PATTERN FLOOR PLAN



TEST PATTERN FLOOR PLAN

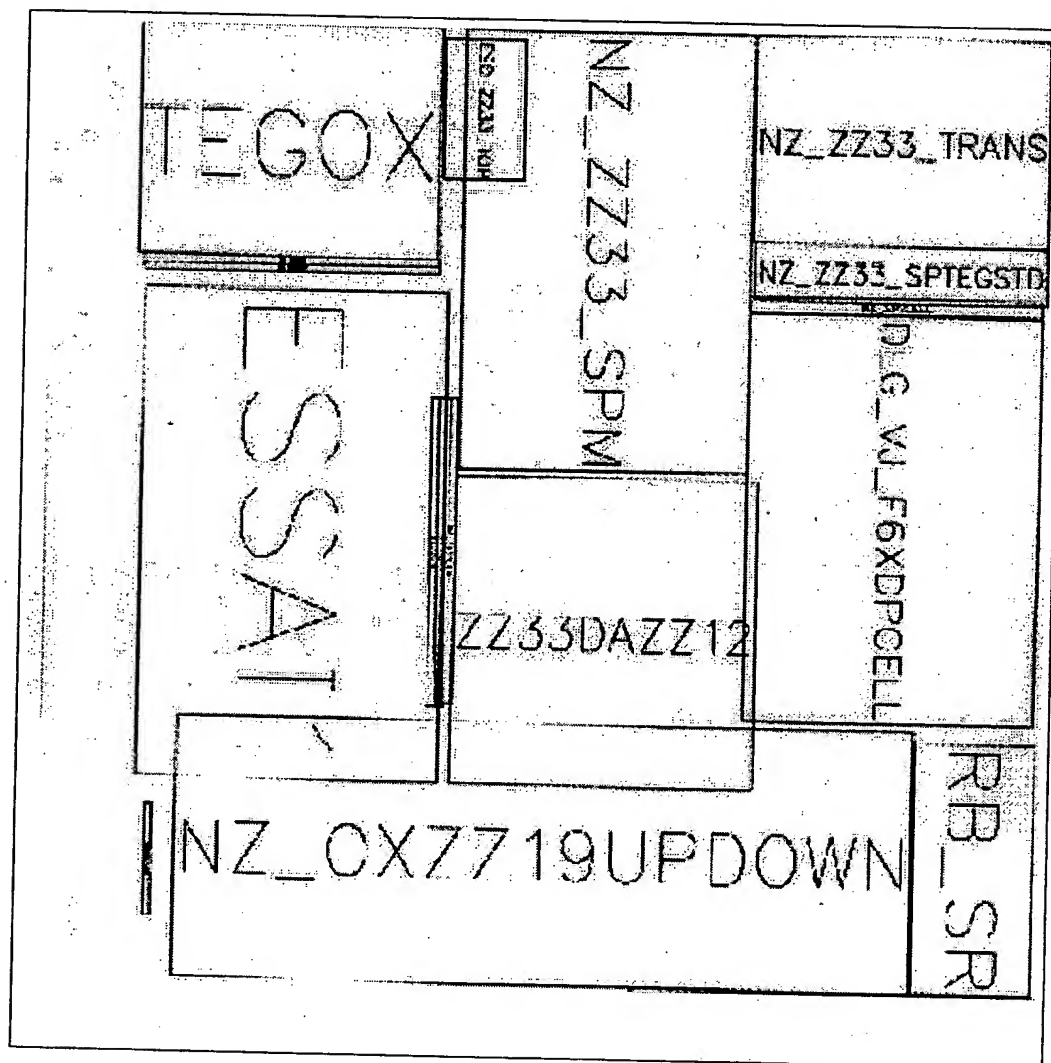


Fig.1 (flat on right side of the page)

ZZ33 TEG1

P-ch LV nat and lvs transistors

PAD	DESCRIPTION	
1	GATE P-CH LV LVS (typ 0.7/0.6)	
2	DRAIN P-CH LV LVS W/L = 10/0.4	
3	DRAIN P-CH LV LVS W/L = 10/0.5	
4	DRAIN P-CH LV LVS W/L = 10/0.6	
5	DRAIN P-CH LV LVS W/L = 10/0.7	
6	DRAIN P-CH LV LVS W/L = 10/0.8	
7	DRAIN P-CH LV LVS W/L = 10/10	
8	DRAIN P-CH LV LVS W/L = 0.6/10	
9	DRAIN P-CH LV LVS W/L = 0.7/10	
10	DRAIN P-CH LV LVS W/L = 0.9/10	
11	DRAIN P-CH LV LVS W/L = 0.7/0.6	
12	DRAIN P-CH LV LVS W/L = 0.65/10	
13	DRAIN P-CH LV LVS W/L = 0.75/10	
14	DRAIN P-CH LV LVS W/L = 10/0.55	
15	DRAIN P-CH LV LVS W/L = 10/0.65	
16	SOURCE	
17	BODY	
18	GATE P-CH LV NAT (typ 0.7/0.6)	
19	DRAIN P-CH LV NAT W/L = 10/0.4	
20	DRAIN P-CH LV NAT W/L = 10/0.5	
21	DRAIN P-CH LV NAT W/L = 10/0.6	
22	DRAIN P-CH LV NAT W/L = 10/0.7	
23	DRAIN P-CH LV NAT W/L = 10/0.8	
24	DRAIN P-CH LV NAT W/L = 10/10	
25	DRAIN P-CH LV NAT W/L = 0.6/10	
26	DRAIN P-CH LV NAT W/L = 0.7/10	
27	DRAIN P-CH LV NAT W/L = 0.9/10	
28	DRAIN P-CH LV NAT W/L = 0.7/0.6	
29	DRAIN P-CH LV NAT W/L = 0.65/10	
30	DRAIN P-CH LV NAT W/L = 0.75/10	
31	DRAIN P-CH LV NAT W/L = 10/0.55	
32	DRAIN P-CH LV NAT W/L = 10/0.65	

ZZ33 TEG2

P-ch LV nat and lvs transistors

PAD	DESCRIPTION	
1	GATE P-CH LV LVS (typ 0.45/0.6)	
2	DRAIN P-CH LV LVS W/L = 10/0.3	
3	DRAIN P-CH LV LVS W/L = 10/0.35	
4	DRAIN P-CH LV LVS W/L = 10/0.45	
5	DRAIN P-CH LV LVS W/L = 10/0.75	
6	DRAIN P-CH LV LVS W/L = 10/0.9	
7	DRAIN P-CH LV LVS W/L = 10/1	
8	DRAIN P-CH LV LVS W/L = 0.4/10	
9	DRAIN P-CH LV LVS W/L = 0.35/10	
10	DRAIN P-CH LV LVS W/L = 0.45/10	
11	DRAIN P-CH LV LVS W/L = 10/0.6 (encl. contact in active d=0.3)	
12	DRAIN P-CH LV LVS W/L = 10/0.6 (encl. contact in active d=0.4)	
13	DRAIN P-CH LV LVS W/L = 10/0.6 (encl. contact in active d=0.5)	
14	DRAIN P-CH LV LVS W/L = 0.45/0.6	
15	DRAIN P-CH LV LVS W/L = 0.55/10	
16	SOURCE	
17	BODY	
18	GATE P-CH LV NAT (typ 0.45/0.6)	
19	DRAIN P-CH LV NAT W/L = 10/0.3	
20	DRAIN P-CH LV NAT W/L = 10/0.35	
21	DRAIN P-CH LV NAT W/L = 10/0.45	
22	DRAIN P-CH LV NAT W/L = 10/0.75	
23	DRAIN P-CH LV NAT W/L = 10/0.9	
24	DRAIN P-CH LV NAT W/L = 10/1	
25	DRAIN P-CH LV NAT W/L = 0.4/10	
26	DRAIN P-CH LV NAT W/L = 0.35/10	
27	DRAIN P-CH LV NAT W/L = 0.45/10	
28	DRAIN P-CH LV NAT W/L = 0.45/0.6	
29	DRAIN P-CH LV NAT W/L = 0.45/0.7	
30	DRAIN P-CH LV NAT W/L = 0.45/0.8	
31	DRAIN P-CH LV NAT W/L = 0.45/0.9	
32	DRAIN P-CH LV NAT W/L = 0.55/10	

ZZ33 TEG3

P-ch HV Drex nat and lvs transistors

PAD	DESCRIPTION	
1	GATE P-CH HV DREX LVS (typ 1.8/1.0)	
2	DRAIN P-CH HV DREX LVS W/L = 10/0.8	
3	DRAIN P-CH HV DREX LVS W/L = 10/0.9	
4	DRAIN P-CH HV DREX LVS W/L = 10/1.0	
5	DRAIN P-CH HV DREX LVS W/L = 10/1.1	
6	DRAIN P-CH HV DREX LVS W/L = 10/1.2	
7	DRAIN P-CH HV DREX LVS W/L = 10/10	
8	DRAIN P-CH HV DREX LVS W/L = 1.7/10	
9	DRAIN P-CH HV DREX LVS W/L = 1.8/10	
10	DRAIN P-CH HV DREX LVS W/L = 2/10	
11	DRAIN P-CH HV DREX LVS W/L = 1.8/1	
12	DRAIN P-CH HV DREX LVS W/L = 1.75/10	
13	DRAIN P-CH HV DREX LVS W/L = 1.95/10	
14	DRAIN P-CH HV DREX LVS W/L = 10/0.95	
15	DRAIN P-CH HV DREX LVS W/L = 10/1.05	
16	SOURCE	
17	BODY	
18	GATE P-CH HV DREX NAT (typ 1.8/1.0)	
19	DRAIN N-CH HV DREX NAT W/L = 10/0.8	
20	DRAIN N-CH HV DREX NAT W/L = 10/0.9	
21	DRAIN N-CH HV DREX NAT W/L = 10/1.0	
22	DRAIN N-CH HV DREX NAT W/L = 10/1.1	
23	DRAIN N-CH HV DREX NAT W/L = 10/1.2	
24	DRAIN N-CH HV DREX NAT W/L = 10/10	
25	DRAIN N-CH HV DREX NAT W/L = 1.7/10	
26	DRAIN N-CH HV DREX NAT W/L = 1.8/10	
27	DRAIN N-CH HV DREX NAT W/L = 2/10	
28	DRAIN N-CH HV DREX NAT W/L = 1.8/1	
29	DRAIN N-CH HV DREX NAT W/L = 1.75/10	
30	DRAIN N-CH HV DREX NAT W/L = 1.95/10	
31	DRAIN N-CH HV DREX NAT W/L = 10/0.95	
32	DRAIN N-CH HV DREX NAT W/L = 10/1.05	

ZZ33 TEG4**P-ch HV Drex nat and lvs transistors**

PAD	DESCRIPTION	
1	GATE P-CH HV DREX LVS (typ 1.8/1.0)	
2	DRAIN P-CH HV DREX LVS W/L = 10/0.55	
3	DRAIN P-CH HV DREX LVS W/L = 10/0.6	
4	DRAIN P-CH HV DREX LVS W/L = 10/0.7	
5	DRAIN P-CH HV DREX LVS W/L = 10/0.75	
6	DRAIN P-CH HV DREX LVS W/L = 10/0.85	
7	DRAIN P-CH HV DREX LVS W/L = 10/1.15	
8	DRAIN P-CH HV DREX LVS W/L = 10/1.25	
9	DRAIN P-CH HV DREX LVS W/L = 10/1.3	
10	DRAIN P-CH HV DREX LVS W/L = 10/4	
11	DRAIN P-CH HV DREX LVS W/L = 10/1.0 (encl. cont. in active d=0.3)	
12	DRAIN P-CH HV DREX LVS W/L = 10/1.0 (encl. cont. in active d=0.4)	
13	DRAIN P-CH HV DREX LVS W/L = 10/1.0 (encl. cont. in active d=0.5)	
14	DRAIN P-CH HV DREX LVS W/L = 10/1.0 (encl. cont. in active d=0.7)	
15	DRAIN P-CH HV DREX LVS W/L = 4/10	
16	SOURCE	
17	BODY	
18	GATE P-CH HV DREX NAT (typ 1.8/1.0)	
19	DRAIN P-CH HV DREX NAT W/L = 10/0.55	
20	DRAIN P-CH HV DREX NAT W/L = 10/0.6	
21	DRAIN P-CH HV DREX NAT W/L = 10/0.7	
22	DRAIN P-CH HV DREX NAT VS W/L = 10/0.75	
23	DRAIN P-CH HV DREX NAT W/L = 10/0.85	
24	DRAIN P-CH HV DREX NAT W/L = 10/1.15	
25	DRAIN P-CH HV DREX NAT W/L = 10/4	
26	DRAIN P-CH HV DREX NAT W/L = 4/10	
27	DRAIN P-CH HV DREX NAT W/L = 10/4	
28	DRAIN P-CH HV DREX NAT W/L = 10/1.0 (encl. cont. in active d=0.3)	
29	DRAIN P-CH HV DREX NAT W/L = 10/1.0 (encl. cont. in active d=0.4)	
30	DRAIN P-CH HV DREX NAT W/L = 10/1.0 (encl. cont. in active d=0.5)	
31	DRAIN P-CH HV DREX NAT W/L = 10/1.0 (encl. cont. in active d=0.7)	
32	DRAIN P-CH HV DREX NAT W/L = 4/10	

ZZ33 TEG5**N-ch HV nat and lvs transistors**

PAD	DESCRIPTION	
1	GATE N-CH HV LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV LVS W/L = 10/0.6	
3	DRAIN N-CH HV LVS W/L = 10/0.7	
4	DRAIN N-CH HV LVS W/L = 10/0.8	
5	DRAIN N-CH HV LVS W/L = 10/0.9	
6	DRAIN N-CH HV LVS W/L = 10/1.0	
7	DRAIN N-CH HV LVS W/L = 10/10	
8	DRAIN N-CH HV LVS W/L = 1.7/10	
9	DRAIN N-CH HV LVS W/L = 1.8/10	
10	DRAIN N-CH HV LVS W/L = 2.0/10	
11	DRAIN N-CH HV LVS W/L = 1.8/0.8	
12	DRAIN N-CH HV LVS W/L = 1.75/10	
13	DRAIN N-CH HV LVS W/L = 1.85/10	
14	DRAIN N-CH HV LVS W/L = 10/0.75	
15	DRAIN N-CH HV LVS W/L = 10/0.85	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV NAT W/L = 10/0.6	
20	DRAIN N-CH HV NAT W/L = 10/0.7	
21	DRAIN N-CH HV NAT W/L = 10/0.8	
22	DRAIN N-CH HV NAT W/L = 10/0.9	
23	DRAIN N-CH HV NAT W/L = 10/1.0	
24	DRAIN N-CH HV NAT W/L = 10/10	
25	DRAIN N-CH HV NAT W/L = 1.7/10	
26	DRAIN N-CH HV NAT W/L = 1.8/10	
27	DRAIN N-CH HV NAT W/L = 2.0/10	
28	DRAIN N-CH HV NAT W/L = 1.8/0.8	
29	DRAIN N-CH HV NAT W/L = 1.75/10	
30	DRAIN N-CH HV NAT W/L = 1.85/10	
31	DRAIN N-CH HV NAT W/L = 10/0.75	
32	DRAIN N-CH HV NAT W/L = 10/0.85	

ZZ33 TEG6**N-ch HV No-Tub nat and lvs transistors**

PAD	DESCRIPTION	
1	GATE N-CH HV NO-TUB LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.6	
3	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.7	
4	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8	
5	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.9	
6	DRAIN N-CH HV NO-TUB LVS W/L = 10/1.0	
7	DRAIN N-CH HV NO-TUB LVS W/L = 10/10	
8	DRAIN N-CH HV NO-TUB LVS W/L = 1.7/10	
9	DRAIN N-CH HV NO-TUB LVS W/L = 1.8/10	
10	DRAIN N-CH HV NO-TUB LVS W/L = 2.0/10	
11	DRAIN N-CH HV NO-TUB LVS W/L = 1.8/0.8	
12	DRAIN N-CH HV NO-TUB LVS W/L = 1.75/10	
13	DRAIN N-CH HV NO-TUB LVS W/L = 1.85/10	
14	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.75	
15	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.85	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.6	
20	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.7	
21	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.8	
22	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.9	
23	DRAIN N-CH HV NO-TUB NAT W/L = 10/1.0	
24	DRAIN N-CH HV NO-TUB NAT W/L = 10/10	
25	DRAIN N-CH HV NO-TUB NAT W/L = 1.7/10	
26	DRAIN N-CH HV NO-TUB NAT W/L = 1.8/10	
27	DRAIN N-CH HV NO-TUB NAT W/L = 2.0/10	
28	DRAIN N-CH HV NO-TUB NAT W/L = 1.8/0.8	
29	DRAIN N-CH HV NO-TUB NAT W/L = 1.75/10	
30	DRAIN N-CH HV NO-TUB NAT W/L = 1.85/10	
31	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.75	
32	DRAIN N-CH HV NO-TUB NAT W/L = 10/0.85	

ZZ33 TEG7**N-ch HV Full Drex nat and LVS transistors**

PAD	DESCRIPTION	
1	GATE N-CH HV DREX LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV DREX LVS W/L = 10/0.6	
3	DRAIN N-CH HV DREX LVS W/L = 10/0.7	
4	DRAIN N-CH HV DREX LVS W/L = 10/0.8	
5	DRAIN N-CH HV DREX LVS W/L = 10/0.9	
6	DRAIN N-CH HV DREX LVS W/L = 10/1.0	
7	DRAIN N-CH HV DREX LVS W/L = 10/10	
8	DRAIN N-CH HV DREX LVS W/L = 1.7/10	
9	DRAIN N-CH HV DREX LVS W/L = 1.8/10	
10	DRAIN N-CH HV DREX LVS W/L = 2.0/10	
11	DRAIN N-CH HV DREX LVS W/L = 1.8/0.8	
12	DRAIN N-CH HV DREX LVS W/L = 1.75/10	
13	DRAIN N-CH HV DREX LVS W/L = 1.85/10	
14	DRAIN N-CH HV DREX LVS W/L = 10/0.75	
15	DRAIN N-CH HV DREX LVS W/L = 10/0.85	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV DREX NAT W/L = 10/0.6	
20	DRAIN N-CH HV DREX NAT W/L = 10/0.7	
21	DRAIN N-CH HV DREX NAT W/L = 10/0.8	
22	DRAIN N-CH HV DREX NAT W/L = 10/0.9	
23	DRAIN N-CH HV DREX NAT W/L = 10/1.0	
24	DRAIN N-CH HV DREX NAT W/L = 10/10	
25	DRAIN N-CH HV DREX NAT W/L = 1.7/10	
26	DRAIN N-CH HV DREX NAT W/L = 1.8/10	
27	DRAIN N-CH HV DREX NAT W/L = 2.0/10	
28	DRAIN N-CH HV DREX NAT W/L = 1.8/0.8	
29	DRAIN N-CH HV DREX NAT W/L = 1.75/10	
30	DRAIN N-CH HV DREX NAT W/L = 1.85/10	
31	DRAIN N-CH HV DREX NAT W/L = 10/0.75	
32	DRAIN N-CH HV DREX NAT W/L = 10/0.85	

ZZ33 TEG8**N-ch HV No-Tub Full Drex nat and LVS transistors**

PAD	DESCRIPTION	
1	GATE N-CH HV NO-TUB DREX LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.6	
3	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.7	
4	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8	
5	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.9	
6	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/1.0	
7	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/10	
8	DRAIN N-CH HV NO-TUB DREX LVS W/L = 1.7/10	
9	DRAIN N-CH HV NO-TUB DREX LVS W/L = 1.8/10	
10	DRAIN N-CH HV NO-TUB DREX LVS W/L = 2.0/10	
11	DRAIN N-CH HV NO-TUB DREX LVS W/L = 1.8/0.8	
12	DRAIN N-CH HV NO-TUB DREX LVS W/L = 1.75/10	
13	DRAIN N-CH HV NO-TUB DREX LVS W/L = 1.85/10	
14	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.75	
15	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.85	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.6	
20	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.7	
21	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8	
22	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.9	
23	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/1.0	
24	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/10	
25	DRAIN N-CH HV NO-TUB DREX NAT W/L = 1.7/10	
26	DRAIN N-CH HV NO-TUB DREX NAT W/L = 1.8/10	
27	DRAIN N-CH HV NO-TUB DREX NAT W/L = 2.0/10	
28	DRAIN N-CH HV NO-TUB DREX NAT W/L = 1.8/0.8	
29	DRAIN N-CH HV NO-TUB DREX NAT W/L = 1.75/10	
30	DRAIN N-CH HV NO-TUB DREX NAT W/L = 1.85/10	
31	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.75	
32	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.85	

ZZ33 TEG9**N-ch HV nat and LVS transistors**

PAD	DESCRIPTION	
1	GATE N-CH HV LVS (typ 1.8/0.8) + NAT full drex (typ 0.45/1)	
2	DRAIN N-CH HV LVS W/L = 10/0.4	
3	DRAIN N-CH HV LVS W/L = 10/0.5	
4	DRAIN N-CH HV LVS W/L = 10/0.55	
5	DRAIN N-CH HV LVS W/L = 10/0.65	
6	DRAIN N-CH HV LVS W/L = 10/0.95	
7	DRAIN N-CH HV LVS W/L = 10/1.05	
8	DRAIN N-CH HV LVS W/L = 10/4	
9	DRAIN N-CH HV LVS W/L = 4/10	
10	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.3)	
11	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.4)	
12	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.5)	
13	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.55)	
14	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.65)	
15	DRAIN N-CH HV LVS W/L = 10/0.8 (encl. cont. in active d=0.7)	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV NAT FULL DREX W/L = 0.35/10	
20	DRAIN N-CH HV NAT FULL DREX W/L = 0.4/10	
21	DRAIN N-CH HV NAT FULL DREX W/L = 0.45/10	
22	DRAIN N-CH HV NAT FULL DREX W/L = 0.55/10	
23	DRAIN N-CH HV NAT FULL DREX W/L = 1/10	
24	DRAIN N-CH HV NAT FULL DREX W/L = 1.2/10	
25	DRAIN N-CH HV NAT FULL DREX W/L = 0.45/1	
26	DRAIN N-CH HV NAT FULL DREX W/L = 0.45/1.2	
27	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 1.0)	
28	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 0.9)	
29	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 0.8)	
30	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 0.7)	
31	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 0.6)	
32	DRAIN N-CH HV NAT FULL DREX W/L = 10/1 (cont. gate dist. 0.5)	

ZZ33 TEG10

N-ch HV No-Tub nat and LVS transistors

PAD	DESCRIPTION
1	GATE N-CH HV NO-TUB LVS (typ 1.8/0.8) + NAT full drex (typ 0.45/1.4)
2	NO-TUB DRAIN N-CH HV NO-TUB LVS W/L = 10/0.4
3	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.5
4	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.55
5	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.65
6	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.95
7	DRAIN N-CH HV NO-TUB LVS W/L = 10/1.05
8	DRAIN N-CH HV NO-TUB LVS W/L = 10/4
9	DRAIN N-CH HV NO-TUB LVS W/L = 4/10
10	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.3)
11	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.4)
12	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.5)
13	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.55)
14	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.65)
15	DRAIN N-CH HV NO-TUB LVS W/L = 10/0.8 (encl. cont. in active d=0.7)
16	SOURCE
17	BODY
18	RING 3-WELL
19	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.2
20	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.3
21	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.4
22	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.5
23	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 0.35/10
24	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 0.4/10
25	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 0.45/10
26	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 0.55/10
27	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 1/10
28	DRAIN N-CH HV NO-TUB NAT FULL DREX W/L = 0.45/1.4
29	N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.4 (cont. gate dist. 0.9)
30	N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.4 (cont. gate dist. 0.8)
31	N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.4 (cont. gate dist. 0.7)
32	N-CH HV NO-TUB NAT FULL DREX W/L = 10/1.4 (cont. gate dist. 0.6)

ZZ33 TEG11

N-ch HV Drex nat and lvs transistors

PAD	DESCRIPTION	
1	GATE N-CH HV DREX LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV DREX LVS W/L = 10/0.4	
3	DRAIN N-CH HV DREX LVS W/L = 10/0.5	
4	DRAIN N-CH HV DREX LVS W/L = 10/0.55	
5	DRAIN N-CH HV DREX LVS W/L = 10/0.65	
6	DRAIN N-CH HV DREX LVS W/L = 10/0.95	
7	DRAIN N-CH HV DREX LVS W/L = 10/1.05	
8	DRAIN N-CH HV DREX LVS W/L = 10/4	
9	DRAIN N-CH HV DREX LVS W/L = 4/10	
10	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.3)	
11	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.4)	
12	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.5)	
13	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.55)	
14	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.65)	
15	DRAIN N-CH HV DREX LVS W/L = 10/0.8 (encl. cont. in active d=0.7)	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV DREX NAT W/L = 10/0.4	
20	DRAIN N-CH HV DREX NAT W/L = 10/0.5	
21	DRAIN N-CH HV DREX NAT W/L = 10/0.55	
22	DRAIN N-CH HV DREX NAT W/L = 10/0.65	
23	DRAIN N-CH HV DREX NAT W/L = 10/0.95	
24	DRAIN N-CH HV DREX NAT W/L = 10/1.05	
25	DRAIN N-CH HV DREX NAT W/L = 10/4	
26	DRAIN N-CH HV DREX NAT W/L = 4/10	
27	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.3)	
28	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.4)	
29	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.5)	
30	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.55)	
31	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.65)	
32	DRAIN N-CH HV DREX NAT W/L = 10/0.8 (encl. cont. in active d=0.7)	

ZZ33 TEG12

N-ch HV Drex No-Tub nat and lvs transistors

PAD	DESCRIPTION	
1	GATE N-CH HV NO-TUB DREX LVS (typ 1.8/0.8) + NAT (typ 1.8/0.8)	
2	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.4	
3	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.5	
4	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.55	
5	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.65	
6	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.95	
7	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/1.05	
8	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/4	
9	DRAIN N-CH HV NO-TUB DREX LVS W/L = 4/10	
10	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.3)	
11	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.4)	
12	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.5)	
13	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.55)	
14	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.65)	
15	DRAIN N-CH HV NO-TUB DREX LVS W/L = 10/0.8 (d=0.7)	
16	SOURCE	
17	BODY	
18	RING 3-WELL	
19	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.4	
20	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.5	
21	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.55	
22	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.65	
23	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.95	
24	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/1.05	
25	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/4	
26	DRAIN N-CH HV NO-TUB DREX NAT W/L = 4/10	
27	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.3)	
28	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.4)	
29	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.5)	
30	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.55)	
31	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.65)	
32	DRAIN N-CH HV NO-TUB DREX NAT W/L = 10/0.8 (d=0.7)	

ZZ33_13: ZZ33 TEG 13 transistor NCH LV NAT and LVS , structure for model card
A = LV LVS Minimum L=0.6 μm Minimum W=0.45 μm

B = LV NAT Minimum L=1.0 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate	GN LV	
2	Drain NCH LV LVS W=10 μm L=0.4 μm	10/0.4 A	
3	Drain NCH LV LVS W=10 μm L=0.5 μm	10/0.5 A	
4	Drain NCH LV LVS W=10 μm L=0.6 μm	10/0.6 A	minimum L
5	Drain NCH LV LVS W=10 μm L=0.7 μm	10/0.7 A	
6	Drain NCH LV LVS W=10 μm L=0.8 μm	10/0.8 A	
7	Drain NCH LV LVS W=10 μm L=10 μm	10/10 A	
8	Drain NCH LV LVS W=0.6 μm L=10 μm	0.6/10 A	
9	Drain NCH LV LVS W=0.7 μm L=10 μm	0.7/10 A	
10	Drain NCH LV LVS W=0.9 μm L=10 μm	0.9/10 A	
11	Drain NCH LV LVS W=0.7 μm L=0.6 μm	0.7/0.6 A	
12	Drain NCH LV LVS W=0.65 μm L=10 μm	.65/10 A	
13	Drain NCH LV LVS W=0.75 μm L=10 μm	.75/10 A	
14	Drain NCH LV LVS W=10 μm L=0.55 μm	10/0.55A	
15	Drain NCH LV LVS W=10 μm L=0.65 μm	10/0.65 A	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH LV NAT W=10 μm L=0.8 μm	10/0.8 B	
20	Drain NCH LV NAT W=10 μm L=0.9 μm	10/0.9 B	
21	Drain NCH LV NAT W=10 μm L=1.0 μm	10/1.0 B	minimum L
22	Drain NCH LV NAT W=10 μm L=1.1 μm	10/1.1 B	
23	Drain NCH LV NAT W=10 μm L=1.2 μm	10/1.2 B	
24	Drain NCH LV NAT W=10 μm L=10 μm	10/10 B	
25	Drain NCH LV NAT W=0.6 μm L=10 μm	0.6/10 B	
26	Drain NCH LV NAT W=0.7 μm L=10 μm	0.7/10 B	
27	Drain NCH LV NAT W=0.9 μm L=10 μm	0.9/10 B	
28	Drain NCH LV NAT W=0.7 μm L=1.0 μm	0.7/1.0 B	
29	Drain NCH LV NAT W=0.65 μm L=10 μm	.65/10 B	
30	Drain NCH LV NAT W=0.75 μm L=10 μm	.75/10 B	
31	Drain NCH LV NAT W=10 μm L=1.05 μm	10/1.05 B	
32	Drain NCH LV NAT W=10 μm L=1.15 μm	10/1.15 B	

ZZ33_14: ZZ33 TEG 14 transistor NCH LV NAT and LVSA = LV LVS Minimum L=0.6 μm Minum W=0.45 μm B = LV NAT Minimum L=1.0 μm Minum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	NOTES
1	Common gate	GN LV	
2	Drain NCH LV LVS W=10 μm L=0.3 μm	10/0.3 A	
3	Drain NCH LV LVS W=10 μm L=0.35 μm	10/0.35 A	
4	Drain NCH LV LVS W=10 μm L=0.45 μm	10/0.45A	
5	Drain NCH LV LVS W=10 μm L=0.75 μm	10/0.75 A	
6	Drain NCH LV LVS W=10 μm L=0.9 μm	10/0.9 A	
7	Drain NCH LV LVS W=10 μm L=1.0 μm	10/1.0 A	
8	Drain NCH LV LVS W=10 μm L=4 μm	10/4 A	
9	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.3)	0.6/10 A .3	for "a"see fig1
10	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.4)	0.6/10 A .4	for "a"see fig1
11	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.5)	0.6/10 A .5	for "a"see fig1
12	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.6)	0.6/10 A .6	for "a"see fig1
13	Drain NCH LV LVS W=1.1 μm L=10 μm	1.1/10 A	
14	Drain NCH LV LVS W=1.2 μm L=10 μm	1.2/10A	
15	Drain NCH LV LVS W=4 μm L=10 μm	4/10 A	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH LV NAT W=10 μm L=0.6 μm	10/0.6 B	
20	Drain NCH LV NAT W=10 μm L=0.7 μm	10/0.7 B	
21	Drain NCH LV NAT W=10 μm L=.75 μm	10/.75 B	
22	Drain NCH LV NAT W=10 μm L=0.85 μm	10/.85B	
23	Drain NCH LV NAT W=10 μm L=0.95 μm	10/.95B	
24	Drain NCH LV NAT W=10 μm L=1.05 μm	10/1.05B	
25	Drain NCH LV NAT W=10 μm L=4 μm	10/0.4 B	
26	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.3)	10/1.0 B .3	for "a"see fig1
27	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.4)	10/1.0 B .4	for "a"see fig1
28	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.5)	10/1.0 B .5	for "a"see fig1
29	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.6)	10/1.0 B .6	for "a"see fig1
30	Drain NCH LV NAT W=1.1 μm L=10 μm	1.1/10 B	
31	Drain NCH LV NAT W=1.2 μm L=10 μm	1.2/10 B	
32	Drain NCH LV NAT W=4 μm L=10 μm	4/10B	

ZZ33_15: ZZ33 TEG 15 transistor NCH LV NAT and LVS NO TUB, structure for model card

A = LV LVS Minimum L=0.6 μm Minimum W=0.45 μm

B = LV NAT Minimum L=1.0 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate	GN LV	
2	Drain NCH LV LVS W=10 μm L=0.4 μm	10/0.4 A	
3	Drain NCH LV LVS W=10 μm L=0.5 μm	10/0.5 A	
4	Drain NCH LV LVS W=10 μm L=0.6 μm	10/0.6 A	minimum L
5	Drain NCH LV LVS W=10 μm L=0.7 μm	10/0.7 A	
6	Drain NCH LV LVS W=10 μm L=0.8 μm	10/0.8 A	
7	Drain NCH LV LVS W=10 μm L=10 μm	10/10 A	
8	Drain NCH LV LVS W=0.6 μm L=10 μm	0.6/10 A	
9	Drain NCH LV LVS W=0.7 μm L=10 μm	0.7/10 A	
10	Drain NCH LV LVS W=0.9 μm L=10 μm	0.9/10 A	
11	Drain NCH LV LVS W=0.7 μm L=0.6 μm	0.7/0.6 A	
12	Drain NCH LV LVS W=0.65 μm L=10 μm	.65/10 A	
13	Drain NCH LV LVS W=0.75 μm L=10 μm	.75/10 A	
14	Drain NCH LV LVS W=10 μm L=0.55 μm	10/0.55A	
15	Drain NCH LV LVS W=10 μm L=0.65 μm	10/0.65 A	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH LV NAT W=10 μm L=0.8 μm	10/0.8 B	
20	Drain NCH LV NAT W=10 μm L=0.9 μm	10/0.9 B	
21	Drain NCH LV NAT W=10 μm L=1.0 μm	10/1.0 B	minimum L
22	Drain NCH LV NAT W=10 μm L=1.1 μm	10/1.1 B	
23	Drain NCH LV NAT W=10 μm L=1.2 μm	10/1.2 B	
24	Drain NCH LV NAT W=10 μm L=10 μm	10/10 B	
25	Drain NCH LV NAT W=0.6 μm L=10 μm	0.6/10 B	
26	Drain NCH LV NAT W=0.7 μm L=10 μm	0.7/10 B	
27	Drain NCH LV NAT W=0.9 μm L=10 μm	0.9/10 B	
28	Drain NCH LV NAT W=0.7 μm L=1.0 μm	0.7/1.0 B	
29	Drain NCH LV NAT W=0.65 μm L=10 μm	.65/10 B	
30	Drain NCH LV NAT W=0.75 μm L=10 μm	.75/10 B	
31	Drain NCH LV NAT W=10 μm L=1.05 μm	10/1.05 B	
32	Drain NCH LV NAT W=10 μm L=1.15 μm	10/1.15 B	

ZZ33_16: ZZ33 TEG 16 transistor NCH LV NAT and LVSA = LV LVS Minimum L=0.6 μm Minimum W=0.45 μm B = LV NAT Minimum L=1.0 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	NOTES
1	Common gate	GN LV	
2	Drain NCH LV LVS W=10 μm L=0.3 μm	10/0.3 A	
3	Drain NCH LV LVS W=10 μm L=0.35 μm	10/0.35 A	
4	Drain NCH LV LVS W=10 μm L=0.45 μm	10/0.45 A	
5	Drain NCH LV LVS W=10 μm L=0.75 μm	10/0.75 A	
6	Drain NCH LV LVS W=10 μm L=0.9 μm	10/0.9 A	
7	Drain NCH LV LVS W=10 μm L=1.0 μm	10/1.0 A	
8	Drain NCH LV LVS W=0.4 μm L=10 μm	0.4/10 A	
9	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.3)	10/0.6 A .3	for "a"see fig1
10	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.4)	10/0.6 A .4	for "a"see fig1
11	Drain NCH LV LVS W=10 μm L=0.6 μm (a=0.5)	10/0.6 A .5	for "a"see fig1
12	Drain NCH LV LVS W=0.45 μm L=0.6 μm	0.45/0.6 A	
13	Drain NCH LV LVS W=0.35 μm L=10 μm	0.35/10 A	
14	Drain NCH LV LVS W=0.45 μm L=10 μm	0.45/10 A	
15	Drain NCH LV LVS W=0.55 μm L=10 μm	0.55/10 A	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH LV NAT W=10 μm L=0.6 μm	10/0.6 B	
20	Drain NCH LV NAT W=10 μm L=0.7 μm	10/0.7 B	
21	Drain NCH LV NAT W=10 μm L=.75 μm	10/.75 B	
22	Drain NCH LV NAT W=10 μm L=0.85 μm	10/.85 B	
23	Drain NCH LV NAT W=10 μm L=0.95 μm	10/.95 B	
24	Drain NCH LV NAT W=10 μm L=1.05 μm	10/1.05 B	
25	Drain NCH LV NAT W=0.4 μm L=10 μm	0.4/10 B	
26	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.3)	10/1.0 B .3	for "a"see fig1
27	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.4)	10/1.0 B .4	for "a"see fig1
28	Drain NCH LV NAT W=10 μm L=1.0 μm (a=0.5)	10/1.0 B .5	for "a"see fig1
29	Drain NCH LV NAT W=0.45 μm L=0.8 μm	0.45/0.8 B	
30	Drain NCH LV NAT W=0.35 μm L=10 μm	0.35/10 B	
31	Drain NCH LV NAT W=0.45 μm L=10 μm	0.45/10 B	
32	Drain NCH LV NAT W=0.55 μm L=10 μm	0.55/10 B	

ZZ33_17: ZZ33 TEG 17 transistor NCH HV Drain extention NAT and LVS , structure for model card

C = HV LVS Minimum L=0.8 μm Minimum W=0.45 μm

D = HV NAT Minimum L=1.8 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate	GN HV	
2	Drain NCH HV LVS W=10 μm L=0.6 μm	10/0.6 D	
3	Drain NCH HV LVS W=10 μm L=0.7 μm	10/0.7 D	
4	Drain NCH HV LVS W=10 μm L=0.8 μm	10/0.8 D	minimum L
5	Drain NCH HV LVS W=10 μm L=0.9 μm	10/0.9 D	
6	Drain NCH HV LVS W=10 μm L=1.0 μm	10/1.0 D	
7	Drain NCH HV LVS W=10 μm L=10 μm	10/10 D	
8	Drain NCH HV LVS W=1.7 μm L=10 μm	1.7/10 D	
9	Drain NCH HV LVS W=1.8 μm L=10 μm	1.8/10 D	
10	Drain NCH HV LVS W=2.0 μm L=10 μm	2.0/10 D	
11	Drain NCH HV LVS W=1.8 μm L=0.8 μm	1.8/0.8D	
12	Drain NCH HV LVS W=1.75 μm L=10 μm	1.75/10 D	
13	Drain NCH HV LVS W=1.85 μm L=10 μm	1.85/10 D	
14	Drain NCH HV LVS W=10 μm L=0.75 μm	10/.75 D	
15	Drain NCH HV LVS W=10 μm L=0.85 μm	10/.85 D	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH HV NAT W=10 μm L=0.6 μm	10/0.6 D	
20	Drain NCH HV NAT W=10 μm L=0.7 μm	10/0.7 D	
21	Drain NCH HV NAT W=10 μm L=0.8 μm	10/0.8 D	minimum L
22	Drain NCH HV NAT W=10 μm L=0.9 μm	10/0.9 D	
23	Drain NCH HV NAT W=10 μm L=1.0 μm	10/1.0 D	
24	Drain NCH HV NAT W=10 μm L=10 μm	10/10 D	
25	Drain NCH HV NAT W=1.7 μm L=10 μm	1.7/10 D	
26	Drain NCH HV NAT W=1.8 μm L=10 μm	1.8/10 D	
27	Drain NCH HV NAT W=2.0 μm L=10 μm	2.0/10 D	
28	Drain NCH HV NAT W=1.8 μm L=0.8 μm	1.8/0.8D	
29	Drain NCH HV NAT W=1.75 μm L=10 μm	1.75/10 D	
30	Drain NCH HV NAT W=1.85 μm L=10 μm	1.85/10 D	
31	Drain NCH HV NAT W=10 μm L=0.75 μm	10/.75 D	
32	Drain NCH HV NAT W=10 μm L=0.85 μm	10/.85 D	

ZZ33_18: ZZ33 TEG 18 transistor NCH HV Drain extention NAT and LVS,
 C = HV LVS Minimum L=0.8 μm Minimum W=0.45 μm
 D = HV NAT Minimum L=1.8 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	NOTES
1	Common gate	GN HV	
2	Drain NCH HV LVS W=10 μm L=0.4 μm	10/0.4 C	
3	Drain NCH HV LVS W=10 μm L=0.5 μm	10/0.5 C	
4	Drain NCH HV LVS W=10 μm L=0.55 μm	10/.55 C	
5	Drain NCH HV LVS W=10 μm L=0.95 μm	10/.95 C	
6	Drain NCH HV LVS W=10 μm L=1.05 μm	10/1.05 C	
7	Drain NCH HV LVS W=10 μm L=1.0 μm	10/10 C	
8	Drain NCH HV LVS W=10 μm L=4 μm	10/4 C	
9	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.3)	0.8/10 C .3	for "a"see fig1
10	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.4)	0.8/10 C .4	for "a"see fig1
11	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.5)	0.8/10 C .5	for "a"see fig1
12	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.55)	0.8/10 C .55	for "a"see fig1
13	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.65)	0.8/10 C .5	for "a"see fig1
14	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.7)	0.8/10 C .7	for "a"see fig1
15	Drain NCH HV LVS W=4 μm L=10 μm	4/10 C	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH HV NAT W=10 μm L=0.4 μm	10/0.4 C	
20	Drain NCH HV NAT W=10 μm L=0.5 μm	10/0.5 C	
21	Drain NCH HV NAT W=10 μm L=0.55 μm	10/.55 C	
22	Drain NCH HV NATW=10 μm L=0.95 μm	10/.95 C	
23	Drain NCH HV NAT W=10 μm L=1.05 μm	10/1.05 C	
24	Drain NCH HV NAT W=10 μm L=1.0 μm	10/10 C	
25	Drain NCH HV NAT W=10 μm L=4 μm	10/4 C	
26	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.3)	0.8/10 C .3	for "a"see fig1
27	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.4)	0.8/10 C .4	for "a"see fig1
28	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.5)	0.8/10 C .5	for "a"see fig1
29	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.55)	0.8/10 C .55	for "a"see fig1
30	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.65)	0.8/10 C .5	for "a"see fig1
31	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.7)	0.8/10 C .7	for "a"see fig1
32	Drain NCH HV NAT W=4 μm L=10 μm	4/10 C	

ZZ33_19: ZZ33 TEG 19 transistor NCH HV Drain extention NAT and LVS No TUB,
structure for model card

C = HV LVS Minimum L=0.8 μm Minimum W=0.45 μm

D = HV NAT Minimum L=1 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate	GN HV	
2	Drain NCH HV LVS W=10 μm L=0.6 μm	10/0.6 D	
3	Drain NCH HV LVS W=10 μm L=0.7 μm	10/0.7 D	
4	Drain NCH HV LVS W=10 μm L=0.8 μm	10/0.8 D	minimum L
5	Drain NCH HV LVS W=10 μm L=0.9 μm	10/0.9 D	
6	Drain NCH HV LVS W=10 μm L=1.0 μm	10/1.0 D	
7	Drain NCH HV LVS W=10 μm L=10 μm	10/10 D	
8	Drain NCH HV LVS W=1.7 μm L=10 μm	1.7/10 D	
9	Drain NCH HV LVS W=1.8 μm L=10 μm	1.8/10 D	
10	Drain NCH HV LVS W=2.0 μm L=10 μm	2.0/10 D	
11	Drain NCH HV LVS W=1.8 μm L=0.8 μm	1.8/0.8D	minimum L
12	Drain NCH HV LVS W=1.75 μm L=10 μm	1.75/10 D	
13	Drain NCH HV LVS W=1.85 μm L=10 μm	1.85/10 D	
14	Drain NCH HV LVS W=10 μm L=0.75 μm	10/.75 D	
15	Drain NCH HV LVS W=10 μm L=0.85 μm	10/.85 D	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH HV NAT W=10 μm L=0.6 μm	10/0.6 D	
20	Drain NCH HV NAT W=10 μm L=0.7 μm	10/0.7 D	
21	Drain NCH HV NAT W=10 μm L=0.8 μm	10/0.8 D	
22	Drain NCH HV NAT W=10 μm L=0.9 μm	10/0.9 D	
23	Drain NCH HV NAT W=10 μm L=1.0 μm	10/1.0 D	
24	Drain NCH HV NAT W=10 μm L=10 μm	10/10 D	
25	Drain NCH HV NAT W=1.7 μm L=10 μm	1.7/10 D	
26	Drain NCH HV NAT W=1.8 μm L=10 μm	1.8/10 D	
27	Drain NCH HV NAT W=2.0 μm L=10 μm	2.0/10 D	
28	Drain NCH HV NAT W=1.8 μm L=0.8 μm	1.8/0.8D	
29	Drain NCH HV NAT W=1.75 μm L=10 μm	1.75/10 D	
30	Drain NCH HV NAT W=1.85 μm L=10 μm	1.85/10 D	
31	Drain NCH HV NAT W=10 μm L=0.75 μm	10/.75 D	
32	Drain NCH HV NAT W=10 μm L=0.85 μm	10/.85 D	

ZZ33_20: ZZ33 TEG 20 transistor NCH HV Drain extention NAT and LVS, NO TUB
 C = HV LVS Minimum L=0.8 μm Minimum W=0.45 μm
 D = HV NAT Minimum L=1 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	NOTES
1	Common gate	GN HV	
2	Drain NCH HV LVS W=10 μm L=0.4 μm	10/0.4 C	
3	Drain NCH HV LVS W=10 μm L=0.5 μm	10/0.5 C	
4	Drain NCH HV LVS W=10 μm L=0.55 μm	10/.55 C	
5	Drain NCH HV LVS W=10 μm L=0.95 μm	10/.95 C	
6	Drain NCH HV LVS W=10 μm L=1.05 μm	10/1.05 C	
7	Drain NCH HV LVS W=10 μm L=1.0 μm	10/10 C	
8	Drain NCH HV LVS W=10 μm L=4 μm	10/4 C	
9	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.3)	0.8/10 C .3	for "a"see fig1
10	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.4)	0.8/10 C .4	for "a"see fig1
11	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.5)	0.8/10 C .5	for "a"see fig1
12	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.55)	0.8/10 C .55	for "a"see fig1
13	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.65)	0.8/10 C .5	for "a"see fig1
14	Drain NCH HV LVS W=10 μm L=0.8 μm (a=0.7)	0.8/10 C .7	for "a"see fig1
15	Drain NCH HV LVS W=4 μm L=10 μm	4/10 C	
16	Common Source	SN	
17	Common Body/well	B	
18	Common Ring to 3 well	3 WELL	
19	Drain NCH HV NAT W=10 μm L=0.4 μm	10/0.4 C	
20	Drain NCH HV NAT W=10 μm L=0.5 μm	10/0.5 C	
21	Drain NCH HV NAT W=10 μm L=0.55 μm	10/.55 C	
22	Drain NCH HV NAT W=10 μm L=0.95 μm	10/.95 C	
23	Drain NCH HV NAT W=10 μm L=1.05 μm	10/1.05 C	
24	Drain NCH HV NAT W=10 μm L=1.0 μm	10/10 C	
25	Drain NCH HV NAT W=10 μm L=4 μm	10/4 C	
26	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.3)	0.8/10 C .3	for "a"see fig1
27	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.4)	0.8/10 C .4	for "a"see fig1
28	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.5)	0.8/10 C .5	for "a"see fig1
29	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.55)	0.8/10 C .55	for "a"see fig1
30	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.65)	0.8/10 C .5	for "a"see fig1
31	Drain NCH HV NAT W=10 μm L=0.8 μm (a=0.7)	0.8/10 C .7	for "a"see fig1
32	Drain NCH HV NAT W=4 μm L=10 μm	4/10 C	

ZZ33_21: ZZ33 TEG 21 transistor PCH HV FULL DREX NAT and LVS with p+ implant around contacts (p+ enclosure in A.A. 0.6 μ m, p+/gate=1.0 μ m, cont.encl. in p+ = 0)

E = HV LVS Minimum L=1.0 μ m Minimum W=0.45 μ m

F = HV NAT Minimum L=1.0 μ m Minimum W=0.45 μ m

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate for transistor with drain 2-15	GP HV	
2	Drain PCH HV LVS W=10 μ m L=0.8 μ m	10/0.8 E	
3	Drain PCH HV LVS W=10 μ m L=0.9 μ m	10/0.9 E	
4	Drain PCH HV LVS W=10 μ m L=1.0 μ m	10/1.0 E	minimum L
5	Drain PCH HV LVS W=10 μ m L=1.1 μ m	10/1.1 E	
6	Drain PCH HV LVS W=10 μ m L=1.2 μ m	10/1.2 E	
7	Drain PCH HV LVS W=10 μ m L=10 μ m	10/10 E	
8	Drain PCH HV LVS W=1.7 μ m L=10 μ m	1.7/10 E	
9	Drain PCH HV LVS W=1.8 μ m L=10 μ m	1.8/10 E	
10	Drain PCH HV LVS W=2.0 μ m L=10 μ m	2.0/10 E	
11	Drain PCH HV LVS W=1.8 μ m L=1.0 μ m	1.8/1.0 E	minimum L
12	Drain PCH HV LVS W=1.75 μ m L=10 μ m	1.75/10 E	
13	Drain PCH HV LVS W=1.95 μ m L=10 μ m	1.95/10 E	
14	Drain PCH HV LVS W=10 μ m L=0.95 μ m	10/0.95 E	
15	Drain PCH HV LVS W=10 μ m L=1.05 μ m	10/1.05 E	
16	Common Source	SP	
17	Common Body/well	B	
18	Common for transistor with drain 19-32	GP HV	
19	Drain PCH HV NAT W=10 μ m L=0.8 μ m	10/0.8 F	
20	Drain PCH HV NAT W=10 μ m L=0.9 μ m	10/0.9 F	
21	Drain PCH HV NAT W=10 μ m L=1.0 μ m	10/1.0 F	minimum L
22	Drain PCH HV NAT W=10 μ m L=1.1 μ m	10/1.1 F	
23	Drain PCH HV NAT W=10 μ m L=1.2 μ m	10/1.2 F	
24	Drain PCH HV NAT W=10 μ m L=10 μ m	10/10 F	
25	Drain PCH HV NAT W=1.7 μ m L=10 μ m	1.7/10 F	
26	Drain PCH HV NAT W=1.8 μ m L=10 μ m	1.8/10 F	
27	Drain PCH HV NAT W=2.0 μ m L=10 μ m	2.0/10 F	
28	Drain PCH HV NAT W=1.8 μ m L=1.0 μ m	1.8/1.0 F	minimum L
29	Drain PCH HV NAT W=1.75 μ m L=10 μ m	1.75/10 F	
30	Drain PCH HV NAT W=1.95 μ m L=10 μ m	1.95/10 F	
31	Drain PCH HV NAT W=10 μ m L=0.95 μ m	10/0.95 F	
32	Drain PCH HV NAT W=10 μ m L=1.05 μ m	10/1.05 F	

ZZ33_22: ZZ33 TEG 22 transistor PCH HV FULL DREX NAT and LVS with p+ implant around contacts (p+ enclosure in A.A. 0.6 μ m typ., p+/gate=1.0 μ m typ., cont.encl. in p+= 0)

E = HV LVS Minimum L=1.0 μ m Minimum W=0.45 μ m

F = HV NAT Minimum L=1.0 μ m Minimum W=0.45 μ m

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate for transistor with drain 2-15	GP HV	
2	Drain PCH HV LVS W=10 μ m L=0.55 μ m	10/0.55 E	
3	Drain PCH HV LVS W=10 μ m L=0.6 μ m	10/0.6 E	
4	Drain PCH HV LVS W=10 μ m L=0.7 μ m	10/0.7 E	
5	Drain PCH HV LVS W=10 μ m L=0.75 μ m	10/.75E	
6	Drain PCH HV LVS W=10 μ m L=0.85 μ m	10/.85 E	
7	Drain PCH HV LVS W=10 μ m L=1.15 μ m	10/1.15 E	
8	Drain PCH HV LVS W=10 μ m L=1.25 μ m	10/1.25 E	
9	Drain PCH HV LVS W=10 μ m L=1.3 μ m	10/1.3 E	
10	Drain PCH HV LVS W=10 μ m L=4 μ m	10/4 E	
11	Drain PCH HV LVS W=10 μ m L=1.0 μ m	10/1.0 E	OV p+ = 0.1
12	Drain PCH HV LVS W=10 μ m L=1.0 μ m	10/1.0 E	OV p+ = 0.2
13	Drain PCH HV LVS W=10 μ m L=1.0 μ m	10/1.0 E	OV p+ = 0.3
14	Drain PCH HV LVS W=10 μ m L=1.0 μ m	10/1.0 E	p+/gate = 0.6
15	Drain PCH HV LVS W=4 μ m L=10 μ m	4/10 E	
16	Common Source	SP	
17	Common Body/well	B	
18	Common for transistor with drain 19-32	GP HV	
19	Drain PCH HV NAT W=10 μ m L=0.55 μ m	10/0.55 F	
20	Drain PCH HV NAT W=10 μ m L=0.6 μ m	10/0.6 F	
21	Drain PCH HV NAT W=10 μ m L=0.7 μ m	10/0.7 F	
22	Drain PCH HV NAT W=10 μ m L=0.75 μ m	10/.75 F	
23	Drain PCH HV NAT W=10 μ m L=0.85 μ m	10/.85 F	
24	Drain PCH HV NAT W=10 μ m L=1.15 μ m	10/1.15 F	
25	Drain PCH HV NAT W=10 μ m L=1.25 μ m	10/1.25 F	
26	Drain PCH HV NAT W=10 μ m L=1.3 μ m	10/1.3 F	
27	Drain PCH HV NAT W=10 μ m L=4 μ m	10/4 F	
28	Drain PCH HV NAT W=10 μ m L=1.0 μ m	10/1.0 F	OV p+ = 0.1
29	Drain PCH HV NAT W=10 μ m L=1.0 μ m	10/1.0 F	OV p+ = 0.2
30	Drain PCH HV NAT W=10 μ m L=1.0 μ m	10/1.0 F	OV p+ = 0.3
31	Drain PCH HV NAT W=10 μ m L=1.0 μ m	10/1.0 F	p+/gate = 0.6
32	Drain PCH HV NAT W=4 μ m L=10 μ m	4/10 F	

ZZ33_23: ZZ33 TEG 23 transistor PCH HV FULL DREX NAT and LVSE = HV LVS Minimum L=1.0 μm Minimum W=0.45 μm F = HV NAT Minimum L=1.0 μm Minimum W=0.45 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate for transistor with drain 2-15	GP HV	
2	Drain PCH HV LVS W=10 μm L=0.8 μm	10/0.8 E	
3	Drain PCH HV LVS W=10 μm L=0.9 μm	10/0.9 E	
4	Drain PCH HV LVS W=10 μm L=1.0 μm	10/1.0 E	minimum L
5	Drain PCH HV LVS W=10 μm L=1.1 μm	10/1.1 E	
6	Drain PCH HV LVS W=10 μm L=1.2 μm	10/1.2 E	
7	Drain PCH HV LVS W=10 μm L=10 μm	10/10 E	
8	Drain PCH HV LVS W=0.35 μm L=10 μm	0.35/10 E	
9	Drain PCH HV LVS W=0.4 μm L=10 μm	0.4/10 E	
10	Drain PCH HV LVS W=0.45 μm L=10 μm	0.45/10 E	
11	Drain PCH HV LVS W=0.45 μm L=1.0 μm	0.45/1.0 E	minimum W,L
12	Drain PCH HV LVS W=0.55 μm L=10 μm	0.55/10 E	
13	Drain PCH HV LVS W=1.0 μm L=10 μm	1/10 E	
14	Drain PCH HV LVS W=10 μm L=0.95 μm	10/95 E	
15	Drain PCH HV LVS W=10 μm L=1.05 μm	10/1.05 E	
16	Common Source	SP	
17	Common Body/well	B	
18	Common for transistor with drain 19-32	GP HV	
19	Drain PCH HV NAT W=10 μm L=0.8 μm	10/0.8 F	
20	Drain PCH HV NAT W=10 μm L=0.9 μm	10/0.9 F	
21	Drain PCH HV NAT W=10 μm L=1.0 μm	10/1.0 F	minimum L
22	Drain PCH HV NAT W=10 μm L=1.1 μm	10/1.1 F	
23	Drain PCH HV NAT W=10 μm L=1.2 μm	10/1.2 F	
24	Drain PCH HV NAT W=10 μm L=10 μm	10/10 F	
25	Drain PCH HV NAT W=0.35 μm L=10 μm	0.35/10 F	
26	Drain PCH HV NAT W=0.4 μm L=10 μm	0.4/10 F	
27	Drain PCH HV NAT W=0.45 μm L=10 μm	0.45/10 F	
28	Drain PCH HV NAT W=0.45 μm L=1.0 μm	0.45/1.0 F	minimum W,L
29	Drain PCH HV NAT W=0.55 μm L=10 μm	0.55/10 F	
30	Drain PCH HV NAT W=1.0 μm L=10 μm	1.0/10 F	
31	Drain PCH HV NAT W=10 μm L=0.95 μm	10/95 F	
32	Drain PCH HV NAT W=10 μm L=1.05 μm	10/1.05 F	

ZZ33_24: ZZ33 TEG 24 transistor PCH HV NAT and LVS Drain extensionE = HV LVS Minimum L=1.0 μm Minum W=1.8 μm F = HV NAT Minimum L=1.0 μm Minum W=1.8 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common gate for transistor with drain 2-15	GP HV	
2	Drain PCH HV LVS W=10 μm L=0.55 μm	10/0.55 E	
3	Drain PCH HV LVS W=10 μm L=0.6 μm	10/0.6 E	
4	Drain PCH HV LVS W=10 μm L=0.7 μm	10/0.7 E	
5	Drain PCH HV LVS W=10 μm L=0.75 μm	10/.75E	
6	Drain PCH HV LVS W=10 μm L=0.85 μm	10/.85 E	
7	Drain PCH HV LVS W=10 μm L=1.15 μm	10/1.15 E	
8	Drain PCH HV LVS W=10 μm L=1.25 μm	10/1.25 E	
9	Drain PCH HV LVS W=10 μm L=1.3 μm	10/1.3 E	
10	Drain PCH HV LVS W=10 μm L=4 μm	10/4 E	
11	Drain PCH HV LVS W=10 μm L=1.0 μm (a=0.3)	10/1.0 E .3	for "a"see fig1
12	Drain PCH HV LVS W=10 μm L=1.0 μm (a=0.4)	10/1.0 E .4	for "a"see fig1
13	Drain PCH HV LVS W=10 μm L=1.0 μm (a=0.5)	10/1.0 E .5	for "a"see fig1
14	Drain PCH HV LVS W=10 μm L=1.0 μm (a=0.7)	10/1.0 E .7	for "a"see fig1
15	Drain PCH HV LVS W=4 μm L=10 μm	4/10 E	
16	Common Source	SP	
17	Common Body/well	B	
18	Common for transistor with drain 19-32	GP HV	
19	Drain PCH HV NAT W=10 μm L=0.55 μm	10/0.55 F	
20	Drain PCH HV NAT W=10 μm L=0.6 μm	10/0.6 F	
21	Drain PCH HV NAT W=10 μm L=0.7 μm	10/0.7 F	
22	Drain PCH HV NAT W=10 μm L=0.75 μm	10/.75 F	
23	Drain PCH HV NAT W=10 μm L=0.85 μm	10/.85 F	
24	Drain PCH HV NAT W=10 μm L=1.15 μm	10/1.15 F	
25	Drain PCH HV NAT W=10 μm L=1.25 μm	10/1.25 F	
26	Drain PCH HV NAT W=10 μm L=1.3 μm	10/1.3 F	
27	Drain PCH HV NAT W=10 μm L=4 μm	10/4 F	
28	Drain PCH HV NAT W=10 μm L=1.0 μm (a=0.3)	10/1.0 F .3	for "a"see fig1
29	Drain PCH HV NAT W=10 μm L=1.0 μm (a=0.4)	10/1.0 F .4	for "a"see fig1
30	Drain PCH HV NAT W=10 μm L=1.0 μm (a=0.5)	10/1.0 F .5	for "a"see fig1
31	Drain PCH HV NAT W=10 μm L=1.0 μm (a=0.7)	10/1.0 F .7	for "a"see fig1
32	Drain PCH HV NAT W=4 μm L=10 μm	4/10 F	

RB_ZENER: Teg for Zener diodes. The zener diode consists of a pn junction formed by the N+ capacitor implant diffusion against P+ S&D diffusion. The standard layout is shown in fig.4a,4b in which capacitor implant diffusion is designed as square area with dimension L ($L=L_1$). In fig.5a,5b the layout of type "B" zener is reported. In this case the P+ diffusion is designed as square area with dimension L ($L=L_1$).

PAD	DESCRIPTION	WRITE on PAD	Notes
1	N+ Zener with $L=2.5\ \mu\text{m}$ and poly plate	CAPA POLY 2.5	see fig. 2
2	P+ Zener with $L=2.5\ \mu\text{m}$ and poly plate	P+	see fig. 2
3	N+ Zener with $L=3\ \mu\text{m}$ and poly plate	CAPA POLY 3	see fig. 2
4	P+ Zener with $L=3\ \mu\text{m}$ and poly plate	P+	see fig. 2
5	Poly contact of Zener diode with N+ and P+ on pad 6 and 7	POLY	
6	N+ Zener with $L=2\ \mu\text{m}$ with poly plate connectable	CAPA 2	
7	P+ Zener with $L=2\ \mu\text{m}$ with poly plate connectable	P+	
8	N+ Zener with $L=2\ \mu\text{m}$ with poly plate	CAPA POLY 2	see fig. 2
9	P+ Zener with $L=2\ \mu\text{m}$ with poly plate	P+	see fig. 2
10	N+ Zener type "B" with $L=3$	CAPA P+=3	see fig. 5a,b
11	P+ Zener type "B" with $L=3$	P+	see fig. 5a,b
12	N+ Zener type "B" with $L=2$	CAPA P+=2	see fig. 5a,b
13	P+ Zener type "B" with $L=2$	P+	see fig. 5a,b
14	N+ Zener with $L=2\ \mu\text{m}$ and $L_1=20\ \mu\text{m}$	CAPA 2/20	see fig. 3
15	P+ Zener with $L=2\ \mu\text{m}$ and $L_1=20\ \mu\text{m}$	P+	see fig. 5a,b
16	N+ of 3 serie conected Zener diode	CAPA 3 ZENER L2	
17	N+ of 4 serie conected Zener diode	CAPA 4 ZENER L2	
18	N+ of 5 serie conected Zener diode	CAPA 5 ZENER L2	
19	P+ for serie conected Zener diode	P+	
20	N+ of 2 serie conected Zener diode	CAPA 2 ZENER L2	
21	N+ Zener with $L=3.5\ \mu\text{m}$	CAPA 3.5	
22	P+ Zener with $L=3.5\ \mu\text{m}$	P+	
23	N+ Zener with $L=2.5\ \mu\text{m}$	CAPA 2.5	
24	P+ Zener with $L=2.5\ \mu\text{m}$	P+	
25	N+ Zener with $L=3.0\ \mu\text{m}$	CAPA 3	
26	P+ Zener with $L=3.0\ \mu\text{m}$	P+	
27	N+ Zener with $L=4.0\ \mu\text{m}$	CAPA 4	
28	P+ Zener with $L=4.0\ \mu\text{m}$	P+	
29	N+ Zener with $L=2.0\ \mu\text{m}$	CAPA 2	
30	P+ Zener with $L=2.0\ \mu\text{m}$	P+	
31	N+ Zener with $L=1.5\ \mu\text{m}$	CAPA 1.5	
32	P+ Zener with $L=1.5\ \mu\text{m}$	P+	

RB_ZENER2: Teg for Zener diode.

PAD	DESCRIPTION	WRITE on PAD	Notes
1	N+ Zener with L=3.5 μm and poly plate	CAPA POLY 3.5	see fig. 2
2	P+ Zener with L=3.5 μm and poly plate	P+	see fig. 2
3	N+ Zener diode with N-well only, without capacitor implant	NWELL, L=11 μm	
4	P+ Zener diode with N-well only, without capacitor implant	P+, L=11 μm	
5	Poly contact of Zener diode with N+ and P+ on pad 6 and 7	POLY	
6	N+ Zener with L=3 μm with poly plate	CAPA 3	see fig. 2
7	P+ Zener with L=3 μm with poly plate	P+	see fig. 2
8	N+ Zener type "B" with L=4 μm and capacitor =well implant	p+ in CAPA P+=4	see fig. 5a,b
9	P+ Zener type "B" with L=4 μm and capacitor =well implant	P+	see fig. 5a,b
10	N+ Zener type "B" with L=3 μm and capacitor =well implant	p+ in CAPA P+=3	see fig. 5a,b
11	P+ Zener type "B" with L=3 μm and capacitor =well implant	P+	see fig. 5a,b
12	N+ Zener type "B" with L=2 μm and capacitor =well implant	p+ in CAPA P+=2	see fig. 5a,b
13	P+ Zener type "B" with L=2 μm and capacitor =well implant	P+	see fig. 5a,b
14	N+ Zener with L=2 μm and L ₁ =21.5 μm	CAPA 2/21.5	see fig. 3
15	P+ Zener with L=2 μm and L ₁ =21.5 μm	P+	see fig. 3
16	N+ Zener with L=2 μm and L ₁ =23 μm	CAPA 2/23	see fig. 3
17	P+ Zener with L=2 μm and L ₁ =23 μm	P+	see fig. 3
18	N+ Zener with L=2 μm and L ₁ =24.5 μm	CAPA 2/24.5	see fig. 3
19	P+ Zener with L=2 μm and L ₁ =24.5 μm	P+	see fig. 3
20	N+ of 3 serie conected Zener diode type "B"	CAPA 3 ZENER P+=2	see fig. 5a,b
21	N+ of 4 serie conected Zener diode type "B"	CAPA 4 ZENER P+=2	see fig. 5a,b
22	N+ of 5 serie conected Zener diode type "B"	CAPA 5 ZENER P+=2	see fig. 5a,b
23	P+ for serie conected Zener diode type "B"	P+	see fig. 5a,b
24	N+ of 2 serie conected Zener diode type "B"	CAPA 2 ZENER P+=2	see fig. 5a,b
25	N+ Zener type "B" with L=2 μm and capacitor =well implant	n+ in p+ (no N-well), n+=4	
26	P+ Zener type "B" with L=2 μm and capacitor =well implant	P+	
27	N+ Zener "B" L=2 and with capacitor =N-well implant	CAPA=W P+=2	see fig. 5a,b
28	P+ Zener "B" L=2 and with capacitor =N-well implant	P+	see fig. 5a,b
29	N+ Zener "B" L=2 and without N-well implant	CAPA=NWELL P+=2	see fig. 5a,b
30	P+ Zener "B" L=2 and without N-well implant	P+	see fig. 5a,b
31	N+ Zener diode with L=4 and contact on N+capacitor implant	CONT CAPA 4	
32	P+ Zener diode with L=4 and contact on N+capacitor implant	P+	

Spreading Resistance Structures

The active area dimensions of each structure are 300x2147 μm

Structures	Layers
P+ S&D in Nwell	17,1,56,2
Capacitor implant and P+ S&D	56,17,3,40,2
Ptub	13,56,2
LVS pch	13,1,2
LVS nch	13,2
P+ Contact in Nwell	56,19,1,2
N+ Contact with N+ S&D in Ptub	56,19,2
Nwell	56,13,1,2
P- LDD	56,57,17,1
N-LDD	56,57,2
P+ S&D	17,56,2
N+S&D	56,2
Capacitor implant	56,13,3,40,2

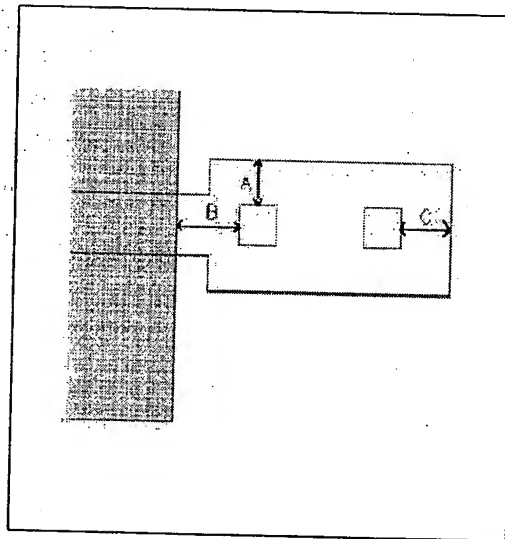


Fig. 1

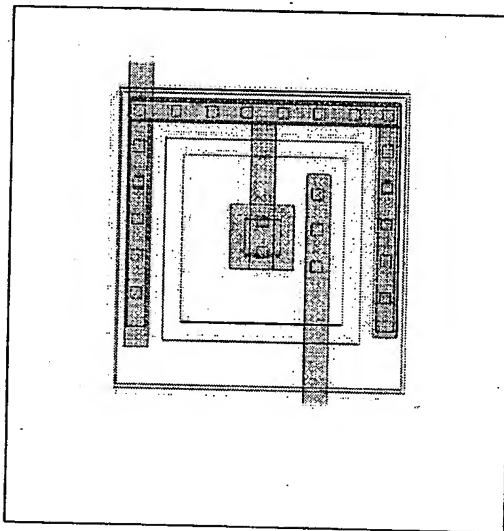


Fig.2

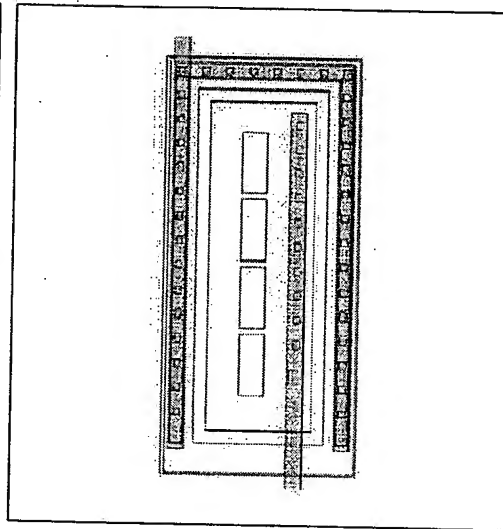


Fig.3

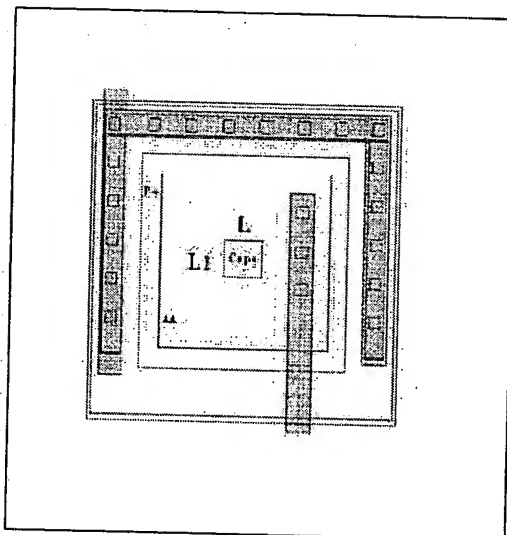


Fig. 4a

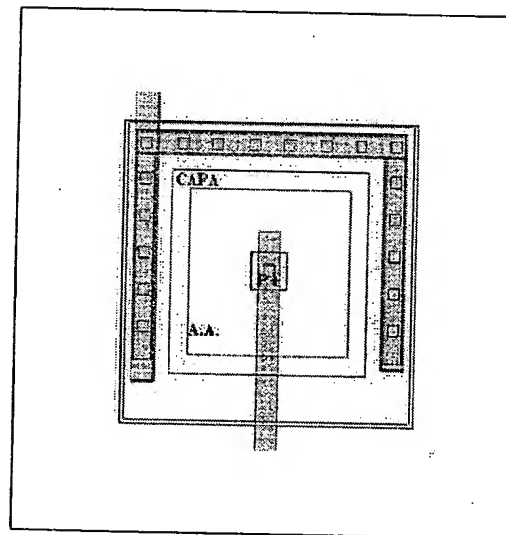


Fig.5a

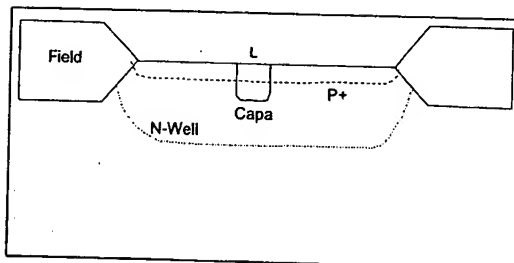


Fig. 4b

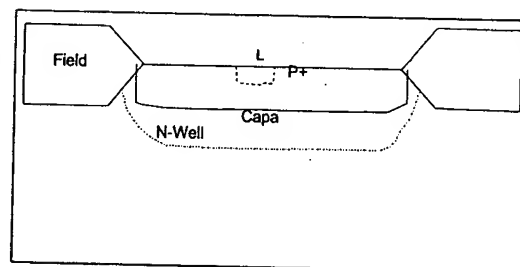


Fig. 5b

ZZ33 TEG SP01
28 μ m² SP cell with different sensing W/L

PAD	DESCRIPTION	
1	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.5/0.4	
2	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.5/0.45	
3	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.5/0.5	
4	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.5/0.55	
5	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.5/0.7	
6	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.6/0.5	
7	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.7/0.4	
8	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.7/0.5	
9	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.7/0.7	
10	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.8/0.45	
11	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.8/0.5	
12	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.8/0.55	
13	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.4	
14	GATE ST1 FOR EVEN BYTE OF SP CELL 28 μ m ²	
15	GATE ST2 FOR ODD BYTE OF SP CELL 28 μ m ²	
16	CONTROL GATE SP CELL 28 μ m ²	
17	SOURCE	
18	BODY	
19	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.45	
20	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.5	
21	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.55	
22	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.6	
23	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.65	
24	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=0.9/0.7	
25	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.0/0.5	
26	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.4	
27	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.45	
28	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.5	
29	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.55	
30	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.6	
31	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.65	
32	DRAIN SP CELL 28 μ m ² WITH SENSING W/L=1.1/0.7	

ZZ33 TEG SP02

28 μm^2 SP equiv. trans. with different sensing W/L

PAD	DESCRIPTION	
1	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.5/0.4	
2	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.5/0.45	
3	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.5/0.5	
4	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.5/0.55	
5	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.5/0.7	
6	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.6/0.5	
7	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.7/0.4	
8	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.7/0.5	
9	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.7/0.7	
10	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.8/0.45	
11	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.8/0.5	
12	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.8/0.55	
13	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.4	
14	GATE ST1 FOR EVEN BYTE OF SP EQ. TR. 28 μm^2	
15	GATE ST2 FOR ODD BYTE OF SP EQ. TR. 28 μm^2	
16	CONTROL GATE SP EQ. TR. 28 μm^2	
17	SOURCE	
18	BODY	
19	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.45	
20	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.5	
21	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.55	
22	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.6	
23	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.65	
24	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=0.9/0.7	
25	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.0/0.5	
26	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.4	
27	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.45	
28	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.5	
29	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.55	
30	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.6	
31	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.65	
32	DRAIN SP EQ. TR. 28 μm^2 WITH SENSING W/L=1.1/0.7	

ZZ33 TEG SP05**28 μm^2 SP cell with different tunnel area and field transistor length**

PAD	DESCRIPTION	
1	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.4/0.4	
2	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.4/0.45	
3	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.4/0.5	
4	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.4/0.55	
5	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.5/0.4	
6	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.5/0.45	
7	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.5/0.5	
8	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.5/0.55	
9	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.6/0.4	
10	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.6/0.45	
11	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.6/0.5	
12	DRAIN SP CELL $28\mu\text{m}^2$ WITH TUNNEL W/L=0.6/0.55	
13	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=0.75/0.5	
14	GATE ST1 FOR EVEN BYTE OF SP CELL $28\mu\text{m}^2$	
15	GATE ST2 FOR ODD BYTE OF SP CELL $28\mu\text{m}^2$	
16	CONTROL GATE SP CELL $28\mu\text{m}^2$	
17	SOURCE	
18	BODY	
19	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=0.8/0.5	
20	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=0.85/0.5	
21	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=0.9/0.5	
22	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=0.95/0.5	
23	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.0/0.5	
24	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.05/0.55	
25	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.1/0.55	
26	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.15/0.55	
27	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.2/0.55	
28	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.25/0.55	
29	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.3/0.5	
30	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.35/0.5	
31	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.4/0.5	
32	DRAIN SP CELL $28\mu\text{m}^2$ WITH FIELD L1/L2=1.4/0.5	

ZZ33 TEG SP06

Sensing and Select transistors for SP $28\mu\text{m}^2$

Pad	DESCRIPTION
1	GATE N-CH LV LVS DREX NO-TUB (SENSING SP typ 0.9/0.5)
2	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/0.4
3	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/0.45
4	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/0.5
5	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/0.6
6	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/0.47
7	DRAIN N-CH LV LVS DREX NO-TUB W/L = 10/10
8	DRAIN N-CH LV LVS DREX NO-TUB W/L = 0.8/10
9	DRAIN N-CH LV LVS DREX NO-TUB W/L = 0.9/10
10	DRAIN N-CH LV LVS DREX NO-TUB W/L = 1.1/10
11	DRAIN N-CH LV LVS DREX NO-TUB W/L = 0.9/0.5
12	SOURCE
13	BODY
14	GATE N-CH HV LVS DREX NO-TUB (SELECT SP typ 1.3/1.0)
15	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/0.8
16	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/0.9
17	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/1.0
18	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/1.1
19	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/1.2
20	DRAIN N-CH HV LVS DREX NO-TUB W/L = 10/10
21	DRAIN N-CH HV LVS DREX NO-TUB W/L = 1.2/10
22	DRAIN N-CH HV LVS DREX NO-TUB W/L = 1.3/10
23	DRAIN N-CH HV LVS DREX NO-TUB W/L = 1.5/10
24	DRAIN N-CH HV LVS DREX NO-TUB W/L = 1.3/1.0
25	Select Transistor 1 (LV oxide)
26	Select Transistor 2 (HV oxide only for Pad 28)
27	Control Gate
28	Drain SP cell 28 μm^2 : tunnel 0.5x0.5, W/L(sens.)=0.9/0.5, coupl.cap.= tun. 1.3x3.55
29	Drain SP cell 28 μm^2 : coupl.cap. 1.85x3.55 (dist. CG-drain=0.9 μm)
30	Drain SP cell 28 μm^2 : coupl.cap. 1.6x3.55 (dist. CG-drain=1.1 μm)
31	Drain SP cell 28 μm^2 : coupl.cap. 1.45x3.55 (dist. CG-drain=1.2 μm)
32	BODY

ZZ33 TEG SP03

28 μm^2 SP cell without Select with different Sensing W/L

PAD	DESCRIPTION	
1	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.5/0.4	
2	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.5/0.45	
3	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.5/0.5	
4	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.5/0.55	
5	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.5/0.7	
6	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.6/0.5	
7	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.7/0.4	
8	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.7/0.5	
9	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.7/0.7	
10	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.8/0.45	
11	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.8/0.5	
12	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.8/0.55	
13	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.4	
14	ST1 DUMMY	
15	ST2 DUMMY	
16	CONTROL GATE SP CELL $28\mu\text{m}^2$	
17	SOURCE	
18	BODY	
19	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.45	
20	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.5	
21	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.55	
22	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.6	
23	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.65	
24	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=0.9/0.7	
25	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.0/0.5	
26	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.4	
27	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.45	
28	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.5	
29	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.55	
30	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.6	
31	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.65	
32	DRAIN SP CELL $28\mu\text{m}^2$ WITH SENSING W/L=1.1/0.7	

ZZ33 TEG SP11
ST in Array dummy for SP $28\mu\text{m}^2$

P-ch HV nat and lvs transistors with a drex/contact misalignment m

PAD	DESCRIPTION	
1	DRAIN ST TYPICAL W/L = 1.3/1.0	
2	DRAIN ST WITH A.A. + 0.1 W/L = 1.4/1.0	
3	DRAIN ST WITH A.A. + 0.2 W/L = 1.5/1.0	
4	DRAIN ST WITH A.A. - 0.1 W/L = 1.2/1.0	
5	DRAIN ST WITH A.A. - 0.2 W/L = 1.1/1.0	
6	DRAIN ST WITH POLY + 0.1 W/L = 1.3/1.1	
7	DRAIN ST WITH POLY + 0.2 W/L = 1.3/1.2	
8	DRAIN ST WITH POLY - 0.1 W/L = 1.3/0.9	
9	DRAIN ST WITH POLY - 0.2 W/L = 1.3/0.8	
10	ST1: GATE FOR ST	
11	S SOURCE	
12	B BODY	
13	GATE P-CH HV LVS W/L = 10/1.0	
14	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0	
15	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.05	
16	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.1	
17	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.15	
18	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.2	
19	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.25	
20	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.3	
21	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.35	
22	DRAIN P-CH HV LVS W/L = 10/1.0 WITH m = 0.4	
23	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0	
24	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.05	
25	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.1	
26	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.15	
27	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.2	
28	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.25	
29	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.3	
30	DRAIN P-CH HV NAT W/L = 10/1.0 WITH m = 0.4	
31	S SOURCE	
32	B n-WELL	

ZZ33 TEG SP07

Matrix (2 Bytes x 11 ST X 2 CG) of SP 28 μ m²

Switch Transistor "tub" in the first three rows

PAD	DESCRIPTION	
1	D10 BITLINE FOR BYTE 1	
2	D11 BITLINE FOR BYTE 1	
3	D12 BITLINE FOR BYTE 1	
4	D13 BITLINE FOR BYTE 1	
5	D14 BITLINE FOR BYTE 1	
6	D15 BITLINE FOR BYTE 1	
7	D16 BITLINE FOR BYTE 1	
8	D17 BITLINE FOR BYTE 1	
9	CG 1 CONTROL GATE 1	
10	CG 0 CONTROL GATE 0	
11	D07 BITLINE FOR BYTE 0	
12	D06 BITLINE FOR BYTE 0	
13	D05 BITLINE FOR BYTE 0	
14	D04 BITLINE FOR BYTE 0	
15	D03 BITLINE FOR BYTE 0	
16	D02 BITLINE FOR BYTE 0	
17	D01 BITLINE FOR BYTE 0	
18	S SOURCE	
19	D00 BITLINE FOR BYTE 0	
20	ST 0	
21	ST 1	
22	ST 3	
23	ST 4	
24	ST 5	
25	ST 6	
26	ST 7	
27	ST 8	
28	ST 9	
29	ST 10	
30	ST 11	
31	B BODY	
32	GND	

Matrix (2 Bytes x 11 ST X 2 CG) of SP 22 μm^2

PAD	DESCRIPTION	
1	D10 BITLINE FOR BYTE 1	
2	D11 BITLINE FOR BYTE 1	
3	D12 BITLINE FOR BYTE 1	
4	D13 BITLINE FOR BYTE 1	
5	D14 BITLINE FOR BYTE 1	
6	D15 BITLINE FOR BYTE 1	
7	D16 BITLINE FOR BYTE 1	
8	D17 BITLINE FOR BYTE 1	
9	CG 1 CONTROL GATE 1	
10	CG 0 CONTROL GATE 0	
11	D07 BITLINE FOR BYTE 0	
12	D06 BITLINE FOR BYTE 0	
13	D05 BITLINE FOR BYTE 0	
14	D04 BITLINE FOR BYTE 0	
15	D03 BITLINE FOR BYTE 0	
16	D02 BITLINE FOR BYTE 0	
17	D01 BITLINE FOR BYTE 0	
18	S SOURCE	
19	D00 BITLINE FOR BYTE 0	
20	ST 0	
21	ST 1	
22	ST 3	
23	ST 4	
24	ST 5	
25	ST 6	
26	ST 7	
27	ST 8	
28	ST 9	
29	ST 10	
30	ST 11	
31	B BODY	
32	GND	

Matrix (2 Bytes x 11 ST X 2 CG) of SP 19 μ m²

PAD	DESCRIPTION	
1	D10 BITLINE FOR BYTE 1	
2	D11 BITLINE FOR BYTE 1	
3	D12 BITLINE FOR BYTE 1	
4	D13 BITLINE FOR BYTE 1	
5	D14 BITLINE FOR BYTE 1	
6	D15 BITLINE FOR BYTE 1	
7	D16 BITLINE FOR BYTE 1	
8	D17 BITLINE FOR BYTE 1	
9	CG 1 CONTROL GATE 1	
10	CG 0 CONTROL GATE 0	
11	D07 BITLINE FOR BYTE 0	
12	D06 BITLINE FOR BYTE 0	
13	D05 BITLINE FOR BYTE 0	
14	D04 BITLINE FOR BYTE 0	
15	D03 BITLINE FOR BYTE 0	
16	D02 BITLINE FOR BYTE 0	
17	D01 BITLINE FOR BYTE 0	
18	S SOURCE	
19	D00 BITLINE FOR BYTE 0	
20	ST 0	
21	ST 1	
22	ST 3	
23	ST 4	
24	ST 5	
25	ST 6	
26	ST 7	
27	ST 8	
28	ST 9	
29	ST 10	
30	ST 11	
31	B BODY	
32	GND	

ZZ33 TEG SP14

ROM Matrix (2 Bytes x 14 Gate)

PAD	DESCRIPTION	
1	D10 DRAIN OF BYTE 1	
2	D11 DRAIN OF BYTE 1	
3	D12 DRAIN OF BYTE 1	
4	D13 DRAIN OF BYTE 1	
5	D14 DRAIN OF BYTE 1	
6	D15 DRAIN OF BYTE 1	
7	D16 DRAIN OF BYTE 1	
8	D17 DRAIN OF BYTE 1	
9	D07 DRAIN OF BYTE 0	
10	D06 DRAIN OF BYTE 0	
11	D05 DRAIN OF BYTE 0	
12	D04 DRAIN OF BYTE 0	
13	D03 DRAIN OF BYTE 0	
14	D02 DRAIN OF BYTE 0	
15	D01 DRAIN OF BYTE 0	
16	D00 DRAIN OF BYTE 0	
17	G0 GATE	
18	G1 GATE	
19	G2 GATE	
20	G3 GATE	
21	G4 GATE	
22	G5 GATE	
23	G6 GATE	
24	G7 GATE	
25	G8 GATE	
26	G9 GATE	
27	G10 GATE	
28	G11 GATE	
29	G12 GATE	
30	G13 GATE	
31	S SOURCE	
32	B BODY	

ZZ33 TEG SP10

Matrix (2 Bytes x 11 ST X 2 CG) of SP 20 μ m²

PAD	DESCRIPTION	
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1	D10 BITLINE FOR BYTE 1	
2	D11 BITLINE FOR BYTE 1	
3	D12 BITLINE FOR BYTE 1	
4	D13 BITLINE FOR BYTE 1	
5	D14 BITLINE FOR BYTE 1	
6	D15 BITLINE FOR BYTE 1	
7	D16 BITLINE FOR BYTE 1	
8	D17 BITLINE FOR BYTE 1	
9	CG 1 CONTROL GATE 1	
10	CG 0 CONTROL GATE 0	
11	D07 BITLINE FOR BYTE 0	
12	D06 BITLINE FOR BYTE 0	
13	D05 BITLINE FOR BYTE 0	
14	D04 BITLINE FOR BYTE 0	
15	D03 BITLINE FOR BYTE 0	
16	D02 BITLINE FOR BYTE 0	
17	D01 BITLINE FOR BYTE 0	
18	S SOURCE	
19	D00 BITLINE FOR BYTE 0	
20	ST 0	
21	ST 1	
22	ST 3	
23	ST 4	
24	ST 5	
25	ST 6	
26	ST 7	
27	ST 8	
28	ST 9	
29	ST 10	
30	ST 11	
31	B BODY	
32	GND	

ZZ33 TEG SP04

Cast SP cell $28\mu\text{m}^2$, $22\mu\text{m}^2$, $19\mu\text{m}^2$, $20\mu\text{m}^2$ + 2 Capacitor

PAD	DESCRIPTION	
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1	CG CONTROL GATE 28 μm^2	
2	BL BITLINE 28 μm^2	
3	ST SELECT 28 μm^2	
4	B BODY 28 μm^2	
5	DUMMY	
6	DUMMY	
7	CG CONTROL GATE 22 μm^2	
8	BL BITLINE 22 μm^2	
9	ST SELECT 22 μm^2	
10	B BODY 22 μm^2	
11	DUMMY	
12	CG CONTROL GATE 19 μm^2	
13	BL BITLINE 19 μm^2	
14	ST SELECT 19 μm^2	
15	B BODY 19 μm^2	
16	DUMMY	
17	CG CONTROL GATE 20 μm^2	
18	BL BITLINE 20 μm^2	
19	ST SELECT 20 μm^2	
20	B BODY 20 μm^2	
21	AA ACTIVE AREA FOR AREA CAPACITOR DP	
22	DUMMY	
23	G GATE FOR AREA CAPACITOR DP	
24	G GATE FOR PERIF. CAPACITOR SP	
25	DUMMY	
26	AA ACTIVE AREA FOR PERIF. CAPACITOR SP	
27	DUMMY	
28	DUMMY	
29	DUMMY	
30	DUMMY	
31	DUMMY	
32	DUMMY	

ZZ33 TEG SP12

Cast equiv. tr. SP 28 μm^2 , 22 μm^2 , 19 μm^2 , 20 μm^2

PAD	DESCRIPTION	
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1	CG CONTROL GATE 28 μm^2	
2	BL BITLINE 28 μm^2	
3	ST SELECT 28 μm^2	
4	B BODY 28 μm^2	
5	DUMMY	
6	DUMMY	
7	CG CONTROL GATE 22 μm^2	
8	BL BITLINE 22 μm^2	
9	ST SELECT 22 μm^2	
10	B BODY 22 μm^2	
11	DUMMY	
12	CG CONTROL GATE 19 μm^2	
13	BL BITLINE 19 μm^2	
14	ST SELECT 19 μm^2	
15	B BODY 19 μm^2	
16	DUMMY	
17	CG CONTROL GATE 20 μm^2	
18	BL BITLINE 20 μm^2	
19	ST SELECT 20 μm^2	
20	B BODY 20 μm^2	
21	DUMMY	
22	DUMMY	
23	DUMMY	
24	DUMMY	
25	DUMMY	
26	DUMMY	
27	DUMMY	
28	DUMMY	
29	DUMMY	
30	DUMMY	
31	DUMMY	
32	DUMMY	

ZZ33 TEG SP13

HV and LV lvs transistors with different contact-gate distance d

PAD	DESCRIPTION	
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1	GATE P-CH HV lvs DREX	
2	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.9	
3	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.8	
4	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.7	
5	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.6	
6	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.5	
7	DRAIN P-CH HV lvs DREX W/L = 10/1.0 d=0.4	
8	SP SOURCE P-CH	
9	BP N-WELL P-CH	
10	GATE P-CH LV lvs	
11	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.8	
12	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.7	
13	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.6	
14	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.5	
15	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.4	
16	DRAIN P-CH LV lvs W/L = 10/0.6 d=0.3	
17	GATE N-CH HV lvs DREX	
18	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.9	
19	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.8	
20	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.7	
21	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.6	
22	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.5	
23	GATE N-CH HV lvs DREX W/L = 10/0.8 d=0.4	
24	SN SOURCE N-CH	
25	BN SUBSTRATE	
26	GATE N-CH LV lvs	
27	GATE N-CH LV lvs W/L = 10/0.6 d=0.8	
28	GATE N-CH LV lvs W/L = 10/0.6 d=0.7	
29	GATE N-CH LV lvs W/L = 10/0.6 d=0.6	
30	GATE N-CH LV lvs W/L = 10/0.6 d=0.5	
31	GATE N-CH LV lvs W/L = 10/0.6 d=0.4	
32	GATE N-CH LV lvs W/L = 10/0.6 d=0.3	

DLGCELL 1.

F6DP Cell (Area=17 μm^2), F6X smallest Cell (Area=7 μm^2), F6X Cell in the PTub and their Equivalent Transistor

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6 L=1 μ m W=0.7 μ m	D F6	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain Trans. Eq. F6 L=1.0 μ m W=0.9 μ m	D F6 TEQ	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain Smallest Cell A=7.0 μ m ²	D AREA 7.0	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain Trans.Eq. Smallest Cell A=7.0 μ m ²	TEQ AREA7.0	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X in the PTUB	F6X PTUB	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain Trans. Eq. of the Cell F6X in the PUB	TEQ PTUB	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 2

Standard F6X Cell (32% shrink): Area=12.76 μ m² (2.9x4.4 μ m) W/L (sensing tr.)=0.5/0.9
W/L (select tr.)=0.8/0.9

and the variations of the sensing transistor length and of the active area width.

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.9 μ m W=0.5 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.8 μ m W=0.5 μ m	D L 0.8	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=1.0 μ m W=0.5 μ m	D L 1.0	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.9 μ m W=0.4 μ m	D W 0.4	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X L=0.9 μ m W=0.6 μ m	D W 0.6	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X L=0.8 μ m W=0.4 μ m	D L 0.8 W 0.4	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELTEQ 2.

Equivalent Transistor of the cells in the teg DLGCELL2

PAD	DESCRIPTION	WRITE on PAD	Notes
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1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.9 μ m W=0.5 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.8 μ m W=0.5 μ m	D L 0.8	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=1.0 μ m W=0.5 μ m	D L 1.0	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.9 μ m W=0.4 μ m	D W 0.4	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X L=0.9 μ m W=0.6 μ m	D W 0.6	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X L=0.8 μ m W=0.4 μ m	D L 0.8 W 0.4	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 3.

Variations of the sensing transistor length and of the active area width of the F6X Cell (32% shrink).

PAD	DESCRIPTION	WRITE on pad	Notes
1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=1 μ m W=0.4 μ m	D L1 W0.4	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=1.0 μ m W=0.6 μ m	D L1 W0.6	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.8 μ m W=0.6 μ m	D L 0.8	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.9 μ m W=0.5 μ m WING=0.85 μ m	D WING 0.85	std wing=0.95
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X with Select Transistor W=1.1 μ m	D AASE1.1	std cell
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X with Select Transistor W=0.5 μ m	D AASEL 0.5	std cell
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELTEQ 3.

Equivalent Transistor of the cells in the teg DLGCELL3

PAD	DESCRIPTION	WRITE on PAD	Notes
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1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=1 μ m W=0.4 μ m	D L1 W0.4	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=1.0 μ m W=0.6 μ m	D L1 W0.6	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.8 μ m W=0.6 μ m	D L 0.8	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.9 μ m W=0.5 μ m WING=0.85 μ m	D WING 0.85	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X with Select transistor W=1.1 μ m	D AASE1.1	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X with Select transistor W=0.5 μ m	D AASEL.5	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 4 (INTER)

Small F6X cell: Area=8.05 μ m² (2.3x3.5) W/L(sensing)=0.4/0.75 W/L(select)=0.8/0.7

Wing=0.75 μ m, Source line=0.6 μ m, P1-P1=0.4 μ m, CG-ST=0.4 μ m

and the variations of the sensing transistor length and of the active area width.

PAD	DESCRIPTION	Write on pad	Notes
1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.75 μ m W=0.4 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.65 μ m W=0.4 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.85 μ m W=0.4 μ m	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.75 μ m W=0.5 μ m	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X (W/L=0.4/0.75): tunnel misaligned +0.1 μ m	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (0.4/0.75): tun. width 0.4 aligned with P1/P2	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELLTEQ 4 (INTER)

Equivalent Transistor of the cells in the teg DLGCELL4.

PAD	DESCRIPTION	Write on pad	Notes
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1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.75 μ m W=0.4 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.65 μ m W=0.4 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.85 μ m W=0.4 μ m	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.75 μ m W=0.5 μ m	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X (W/L=0.4/0.75): tunnel misaligned +0.1 μ m	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (0.4/0.75): tun. width 0.4 aligned with P1/P2	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 5 (MILAN)

Advanced F6X cell (36% shrink): Area=10.4 μ m² (2.4x6 μ m) W/L (sensing tr.)=0.4/0.8
W/L(select tr.)=0.8/0.8 Wing=0.90 μ m and the variations of the sensing transistor length and of the active area width.

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common body	BODY	
2	Common Source	SOURCE	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.8 μ m W=0.4 μ m	D AREA 10.4	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.7 μ m W=0.4 μ m	D L 0.7	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.9 μ m W=0.4 μ m	D L 0.9	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.8 μ m W=0.3 μ m	D W 0.3	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X L=0.8 μ m W=0.5 μ m	D W 0.5	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X small with Sel.Trans. W=1.1 μ m	D AASEL1.1	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELLTEQ 5 (MILAN)

Equivalent Transistor of the cells in the teg DLGCELL5

PAD	DESCRIPTION	WRITE on PAD	Notes
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1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.8 μ m W=0.4 μ m	D AREA 10.4	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.7 μ m W=0.4 μ m	D L 0.7	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.9 μ m W=0.4 μ m	D L 0.9	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X L=0.8 μ m W=0.3 μ m	D W 0.3	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X L=0.8 μ m W=0.5 μ m	D W 0.5	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X small with Sel.Trans. W=1.1 μ m	D AASEL1.1	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 6

F6X Byte and Small F6X Byte and Standard Cell F6X without select transistor

PAD	DESCRIPTION	WRITE on PAD	Notes
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1	Body of F6X and Small F6X Bytes	B	
2	Source of F6X Byte	S	
3	First Drain of F6X Byte	D1	W/L=.8/.9
4	Second Drain of F6X Byte	D2	
5	Third Drain of F6X Byte	D3	
6	Fourth Drain of F6X Byte	D4	
7	Fifth Drain of F6X Byte	D5	
8	Sixth Drain of F6X Byte	D6	
9	Seventh Drain of F6X Byte	D7	
10	Eighth Drain of F6X Byte	D8	
11	Control Gate down of F6X Byte	CGB	
12	Select transistor down of F6X Byte	SB	
13	Select transistor upper of F6X Byte	SA	
14	Control Gate upper of F6X Byte	CGA	
15	First Drain Small F6X Byte	D1	W/L=.6/.8
16	Second Drain of Small F6X Byte	D2	
17	Third Drain of Small F6X Byte	D3	
18	Fourth Drain of Small F6X Byte	D4	
19	Fifth Drain of Small F6X Byte	D5	
20	Sixth Drain of Small F6X Byte	D6	
21	Seventh Drain of Small F6X Byte	D7	
22	Eighth Drain of Small F6X Byte	D8	
23	Control Gate down of Small F6X Byte	CGB	
24	Select transistor down of Small F6X Byte	SB	
25	Select transistor upper of Small F6X Byte	SA	
26	Control Gate upper of Small F6X Byte	CGA	
27	Source of Small F6x Byte	S	
28	Drain F6X W/L=0.8/0.9 without Sel. Trans.	F6X NO SEL	
29	Source	S	
30	Control Gate down	CGB	
31	Control Gate upper	CGA	
32	Body of Cell without Select transistor	B	

DLGCELL7

Advanced F6X Byte and Advanced F6X Bytone. Bytone is an all addressing byte.

PAD	DESCRIPTION	WRITE on PAD	Notes
-----	-------------	--------------	-------

1	Common body	B	
2	Source of Byte	S	
3	First Drain of Advanced F6X Byte	D1	W/L=.5/.8
4	Second Drain of Advanced F6X Byte	D2	
5	Third Drain of Advanced F6X Byte	D3	
6	Fourth Drain of Advanced F6X Byte	D4	
7	Fifth Drain of Advanced F6X Byte	D5	
8	Sixth Drain of Advanced F6X Byte	D6	
9	Seventh Drain of Advanced F6X Byte	D7	
10	Eighth Drain of Advanced F6X Byte	D8	
11	Control Gate down	CGB	
12	Select transistor down	SB	
13	Select transistor upper	SA	
14	Control Gate upper	CGA	
15	External source of Bytone	S	
16	First Drain Advanced F6X Bytone	D1	W/L=.5/.8
17	Second Drain of Advanced F6X Bytone	D2	
18	Third Drain of Advanced F6X Bytone	D3	
19	Fourth Drain of Advanced F6X Bytone	D4	
20	Fifth Drain of Advanced F6X Bytone	D5	
21	Sixth Drain of Advanced F6X Bytone	D6	
22	Seventh Drain of Advanced F6X Bytone	D7	
23	Eighth Drain Advanced F6X Bytone	D8	
24	Control Gate down	CGB	
25	Select transistor down	SB	
26	Select transistor upper	SA	
27	Control Gate upper	CGA	
28	Source First and second cells of byte	S1	
29	Source of third and fourth cells of byte	S2	
30	Source of fifth and sixth cells of byte	S3	
31	Source of seventh and eighth cells of byte	S4	
32	Contact to source line of Bytone		

DLGCELL 8

F6X Bytone and Small F6X Bytone. Bytone is an all addressing byte.

Not modified cell in this revision.

PAD	DESCRIPTION	WRITE on PAD	Notes
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1	Common body	B	
2	External Source	S	
3	First Drain of F6X Bytone	D1	W/L=.8/.9
4	Second Drain of F6X Bytone	D2	
5	Third Drain of F6X Bytone	D3	
6	Fourth Drain of F6X Bytone	D4	
7	Fifth Drain of F6X Bytone	D5	
8	Sixth Drain of F6X Bytone	D6	
9	Seventh Drain of F6X Bytone	D7	
10	Eighth Drain of F6X Bytone	D8	
11	Control Gate down	CGB	
12	Select transistor down	SB	
13	Select transistor upper	SA	
14	Control Gate upper	CGA	
15	First and second sources of bytes	S1	
16	Third and fourth sources of bytes	S2	
17	Fifth and sixth sources of bytes	S3	
18	Seventh and eighth sources of bytes	S4	
19			
20	First Drain of Small F6X bytone	D1	W/L=.6/.8
21	Second Drain of Small F6X Bytone	D2	
22	Third Drain of Small F6X Bytone	D3	
23	Fourth Drain of Small F6X Bytone	D4	
24	Fifth Drain of Small F6X Bytone	D5	
25	Sixth Drain of Small F6X Bytone	D6	
26	Seventh Drain of Small F6X Bytone	D7	
27	Eighth drain of Small F6X bytone	D8	
28	Control Gate down	CGB	
29	Select transistor down	SB	
30	Select transistor upper	SA	
31	Control Gate upper	CGA	
32	External source	S	

DLGCELL 9

F6X Cast (512K), Advanced F6X Cast (512K), Small F6X Cast (512K) and noDPCC F6X Cast (512K)

NODPCC cell and its Equivalent transistor.

Poly1 and Poly2 Resistors.

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Drain of F6X CAST	D F6X	
2	Select transistor of F6X CAST	ST F6X	
3	Control Gate of F6X CAST	CG F6X	
4	Source of F6X CAST	S F6X	
5	Drain of Small F6X CAST	D INTER	
6	Select transistor of Small F6X CAST	ST	
7	Control Gate of Small F6X CAST	CG	
8	Source of Small F6X CAST	S	
9	Contact to Poly2 res. 1.2x60µm		
10	Common Contact to Poly2 res.		
11	Contact to Poly2 res. 0.6x60µm		
12	Contact to Poly1 res. 0.8x80µm		
13	Contact to Poly1 res. 0.8x80µm	S nodpcc	
14	Select transistor of NODPCC F6X CAST	CG nodpcc	
15	Body of F6X, Small and Nodpcc CAST	BODY	
16	Drain of NODPCC F6X CAST	D nodpcc	
17	Select transistor of NODPCC F6X CAST	ST nodpcc	
18	Drain of Advanced F6X CAST	D MILAN	
19	Select transistor of Advanced F6X CAST	ST	
20	Control Gate of Advanced F6X CAST	CG	
21	Source of Advanced F6X CAST	S	
22	Drain of NODPCC F6X Cell	D	
23	Source of NODPCC F6X Cell	S	
24	Select transistor down of NODPCC F6X Cell	STB	
25	Control gate down of NODPCC F6X Cell	CGB	
26	Control gate upper of NODPCC F6X Cell	CGA	
27	Select transistor upper of NODPCC F6X Cell	STA	
28	Drain of NODPCC F6X Equiv. Trans.	D	
29	Source of NODPCC F6X Equiv. Trans.	S	
30	Control gate of NODPCC F6X Equiv. Trans.	CG	
31	Select transistor of NODPCC F6X Equiv. Trans	ST	
32	Source of the NODPCC F6X CAST		

DLGCELL10

Advanced F6X Cell (36% shrink) W/L (sensing tr.)=0.4/0.8 W/L(select tr.)=0.8/0.8

Wing=0.90µm with capa implant on the source line.

PAD	DESCRIPTION	WRITE on pad	Notes
-----	-------------	--------------	-------

1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X (std): capa=0.6 μ m, capa-capa dist.=1.1 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X (std): capa=0.4 μ m, capa-capa dist.=1.2 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X (std): capa=0.8 μ m, capa-capa dist.=1.0 μ m	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X (std): capa=0.6 μ m, W(sensing)=0.5 μ m	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X (std): capa=0.6 μ m, L(CG) -0.1 μ m	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (std): capa=0.6 μ m, L(CG) +0.1 μ m	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELLTEQ10

Equivalent Transistor of Cells in DLGCELL10

PAD	DESCRIPTION	WRITE on pad	Notes
1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X (std): capa=0.6 μ m, capa-capa dist.=1.1 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X(std): capa=0.4 μ m, capa-capa dist.=1.2 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X (std): capa=0.8 μ m, capa-capa dist.=1.0 μ m	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X(std): capa=0.6 μ m, W(sensing)=0.5 μ m	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X (std): capa=0.6 μ m, L(CG) -0.1 μ m	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (std): capa=0.6 μ m, L(CG) +0.1 μ m	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 11

Advanced F6X Cell (36% shrink) W/L (sensing tr.)=0.4/0.8 W/L(select tr.)=0.8/0.8:
dimensions variation.

PAD	DESCRIPTION	WRITE on pad	Notes
-----	-------------	--------------	-------

1	Common body	BODY	
2	Common Source	SOURCE	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.9 μ m W=0.5 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.7 μ m W=0.5 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X W/L=0.4/0.8 μ m: tunnel misaligned +0.1	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X W/L=0.4/0.8 μ m: capa misaligned -0.1	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X W/L=0.4/0.8 μ m: tunnel enclosed in P2	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (std): capa-implant on source line/P1 trenches	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELLTEQ11

Equivalent Transistor of Cells in DLGCELL11

PAD	DESCRIPTION	WRITE on pad	Notes
-----	-------------	--------------	-------

1	Common body	BODY	
2	Common Source	SOURCE	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.9 μ m W=0.5 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.7 μ m W=0.5 μ m	D	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X W/L=0.4/0.8 μ m: tunnel misaligned +0.1	D	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X W/L=0.4/0.8 μ m: capa misaligned -0.1	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X W/L=0.4/0.8 μ m: tunnel enclosed in P2	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain F6X (std): capa-implant on source line/P1 trenches	D	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL12

F6X Miscellanea.

PAD	DESCRIPTION	WRITE on PAD	Notes
-----	-------------	--------------	-------

1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X with Select all DPCC	D NONO1	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain Equivalent transistor	D NONO1	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X	D Vias on CG	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X NoDPCC without Sel.Trans.	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain Advanced F6X without Sel.Trans.	D Milan NOSEL	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain Small F6X without Sel Trans.	D Inter NOSEL	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGCELL 13

No self-aligned F6X Cell : Area=12.2 μm^2 W/L(sensing tr.)=0.5/0.8 W/L(select tr.)=0.8/0.8 and the variations of the sensing transistor length and of the active area width.

Tunnel=0.4x1.5 μm , wings=1 μm , source line=0.8 μm

PAD	DESCRIPTION	WRITE on PAD	Notes
-----	-------------	--------------	-------

1	Common body	B	
2	Common Source	S	
3	Select transistor upper	STA	
4	Control Gate upper	CGA	
5	Drain F6X L=0.8 μ m W=0.5 μ m	D	
6	Select transistor down	STB	
7	Control Gate down	CGB	
8	Select transistor upper	STA	
9	Control Gate upper	CGA	
10	Drain F6X L=0.9 μ m W=0.5 μ m	D L 0.9	
11	Select transistor down	STB	
12	Control Gate down	CGB	
13	Select transistor upper	STA	
14	Control Gate upper	CGA	
15	Drain F6X L=0.7 μ m W=0.5 μ m	D L 0.7	
16	Select transistor down	STB	
17	Control Gate down	CGB	
18	Select transistor upper	STA	
19	Control Gate upper	CGA	
20	Drain F6X (std): poly2 misaligned +0.2 μ m	D	
21	Select transistor down	STB	
22	Control Gate down	CGB	
23	Select transistor upper	STA	
24	Control Gate upper	CGA	
25	Drain F6X (std): tunnel misaligned +0.2 μ m	D	
26	Select transistor down	STB	
27	Control Gate down	CGB	
28	Select transistor upper	STA	
29	Control Gate upper	CGA	
30	Drain Equivalent Transistor L=0.8 μ m W=0.5 μ m	D L 0.8 W 0.7	
31	Select transistor down	STB	
32	Control Gate down	CGB	

DLGSELECT

Select transistors in array dummy.

PAD	DESCRIPTION	WRITE on PAD	Notes
1	Common body	B	

2	Common Source	S	
3	Common Gate	G	
4	Select transistor W/L = 10/10		
5	Select transistor W/L = 10/0.9		
6	Select transistor W/L = 0.8/10		
7	F6X Select transistor W/L = 0.8/0.9		
8	F6X Select transistor W/L = 0.7/0.9		
9	F6X Select transistor W/L = 0.9/0.9		
10	F6X Select transistor W/L = 0.8/0.8		
11	F6X Select transistor W/L = 0.8/1.0		
12	F6X Select transistor capa/poly distance=0.25um		W/L=.8/.9
13	F6X Select transistor capa/poly distance=0.35um		W/L=.8/.9
14	F6X Select transistor capa/poly distance=0.45um		W/L=.8/.9
15	F6X Select transistor capa/poly distance=0.15um		W/L=.8/.9
16	Advanced F6X Select transistor W/L = 0.6/0.8		
17	Advanced F6X Select transistor W/L = 0.5/0.8		
18	Advanced F6X Select transistor W/L = 0.7/0.8		
19	Advanced F6X Select transistor W/L = 0.6/0.7		
20	Advanced F6X Select transistor W/L = 0.6/0.9		
21	Small F6X Select transistor W/L = 1.0/0.7		
22	Source Resistance "old" (1 byte)		
23	Small F6X Select transistor W/L = 0.9/0.7		
24	Small F6X Select transistor W/L = 1.0/0.6		
25	Small F6X Select transistor W/L = 1.0/0.8		
26	F6X Select transistor W/L = 1.4/0.9		
27	Source Resistance "standard" (1 byte)		
28	Source Resistance "capa" (1 byte)		
29	Select transistor no DPCC		W/L=.8/.9
30	F6X Select transistor in the P-TUB		W/L=.8/.9
31	Advanced F6X Select transistor in the P-TUB		W/L=.6/.8
32	Source Resistance with capa-implant on source line/P1 trenches		

Part 2)

This document is an updated description of the test structures for oxide characterisation of the test pattern ZZ33. Only TEGs A, B and C have been completely reviewed. Two area capacitor (HV and LV, 1mm² area) on capa implant have been added to NZ_ZZ33_SPM module.

The following corrections have been made on the other TEGs:

TEG D and TEG F: arrays have been corrected as HV oxide, natural, tub, $W(A.A.)=0.4\mu\text{m}$, tunnel= $0.7\times 1.5\mu\text{m}$

TEG F:

- Perimeter tunnel capacitor $(0.4\times 1.5\mu\text{m})\times 24$ (single array) $\times 250$ (rows) $\times 40$ (columns). $A=1.44\text{e-}3\text{ cm}^2$, Perimeter on field= $(2\times 1.5\mu\text{m})\times 24$ (single array) $\times 250$ (rows) $\times 40$ (columns)= 72cm , Perimeter self-aligned on field= $(0.4\times 2\mu\text{m})\times 24$ (single array) $\times 250$ (rows) $\times 40$ (columns)= 19.2cm
- Perimeter tunnel capacitor with half periphery (250 rows \times 20 columns). Perimeter on field= 36cm , $A=0.9\text{e-}3\text{ cm}^2$
- Pad 29-30-31: 1 capacitor $L=1\mu\text{m}$ (0.5 tunnel), $W=0.4$
1 capacitor $L=1\mu\text{m}$ (HV oxide), $W=0.4$

TEG A

6 structures are present on this TEG.

- The first structure is a memory array of standart F6X cells without select transistors. The matrix is made up by 128×64 cells. The array has three pads collecting all the drains, sources and gates of each cell. The dimensions of the cell are as follows :

Poly Length= $1.7\mu\text{m}$

Active width= $0.9\mu\text{m}$

Tunnel window= $0.5\times 0.5\mu\text{m}^2$

Tunnel window/gate edge distance= $0.15\mu\text{m}$

Tunnel window/capacitor implant= $0.15\mu\text{m}$

- 4 identical capacitors for tunnel oxide characterisation. Each capacitor is made up by an array of 10×10 basic structures. Tunnel oxide region is defined in a LV oxide area over a substrate doped by the capacitor implant. The poly contact is taken over a field oxide square ($16\times 16\mu\text{m}^2$) grown in the middle of the active area of the basic structure ($106\times 106\mu\text{m}^2$). The distance between tunnel mask and active area mask is $2\mu\text{m}$.

The area of each basic structure is : $100\times (102^2-20^2)=1\ 004\ 000\mu\text{m}^2\sim 1\text{e-}2\text{ cm}^2$

The total length of the periphery between LV and tunnel oxide is :

$$100\times [(4\times 102)+(4\times 20)]=48\ 800\mu\text{m}\sim 4.88\text{e-}2\text{ cm}$$

With this structure also ONO can be evaluated. The total ONO area is $1.11215\text{e-}2\text{ cm}^2$ while the total length of the self aligned ONO periphery is $4.668\text{e-}2\text{ cm}$.

- The last structure is similar to the previous ones with 5×10 basic element.

TEG A

PAD	STRUCTURES	DESCRIPTION
1	128×64 Standart F6X Cells without select	Source
2	Tunnel window= $0.5\times 0.5\mu\text{m}^2$	Gate
3		Drain

4	CAP Tunnel Area $1e-2 \text{ cm}^2$	P1
5		N+ SUB
6	CAP ONO Area $1.1e-2 \text{ cm}^2$	P2
7		
8		
9		
10	CAP Tunnel Area $1e-2 \text{ cm}^2$	P1
11		N+ SUB
12	CAP ONO Area $1.1e-2 \text{ cm}^2$	P2
13		
14		
15		
16	CAP Tunnel Area $1e-2 \text{ cm}^2$	P1
17		N+ SUB
18	CAP ONO Area $1.1e-2 \text{ cm}^2$	P2
19		
20		
21		
22	CAP Tunnel Area $1e-2 \text{ cm}^2$	P1
23		N+ SUB
24	CAP ONO Area $1.1e-2 \text{ cm}^2$	P2
25		
26		
27		
28	CAP Tunnel Area $5e-3 \text{ cm}^2$	P1
29		N+ SUB
30	CAP ONO Area $5.5e-3 \text{ cm}^2$	P2
31	GROUND	GND
32	GROUND	GND

TEG B

The 8 first test structures are arrays of 128x64 select transistors. Each array has three pads collecting all the gates, drains and sources. The active width is $1 \mu\text{m}$ for all the arrays.

Structures 9 and 11 are respectively made up by 10 and 50 basic structures already described in TEG A.

Structure 10 is made by 10 squares of polysilicon in order to measure the sheet resistance of the poly1.

TEG B

PAD	STRUCTURES	DESCRIPTION
1	#1 Poly length=0.9 μm	Source
2	#1	Gate
3	#1	Drain
4	#2 Poly length=1 μm	Source

5	#2	Gate
6	#2	Drain
7	#3 Poly length=1.1 μm	Source
8	#3	Gate
9	#3	Drain
10	#4 Distance of implant capacitor over the source	Source
11	#4 from the gate = 0.3 μm	Gate
12	#4	Drain
13	#5 Distance of implant capacitor over the source	Source
14	#5 from the gate = 0.4 μm	Gate
15	#5	Drain
16	#6 Distance of implant capacitor over the source	Source
17	#6 from the gate=0.5 μm	Gate
18	#6	Drain
19	#7 Distance of implant capacitor over the source	Source
20	#7 from the gate=0.6 μm	Gate
21	#7	Drain
22	#8 Distance of implant capacitor over the source	Source
23	#8 from the gate=0.7 μm	Gate
24	#8	Drain
25	#9CAP Tunnel Area=1e-3 cm2 # 9	P1
26	#9	SUB
27	#9	P2
28	#10 Poly1 resistor #10	GND
29	#10	R1
30	#11 CAP Tunnel Area=5e-3 cm2 # 11	SUB
31	#11	P1
32	#11	P2

TEG C

In this TEG, 8 arrays of "cell like" structures (i.e. poly strip under which a tunnel region is opened in a LV area) are coupled with "transistor like" structures (i.e. poly strip under which a LV oxide is grown). The polysilicon gates of "cell like" transistor like" structures are independent. Both tunnel and LV oxide are grown on n+ implant capacitor. Each array is made up by 128x64 structures. The poly length of the "transistor like" and "cell like" structures is 1 μm for all the arrays. For the structure number 6, a tunnel oxide is grown under the polysilicon

gate of the "transistor-like" structure. The different geometries of each test structure are summarised in table 1 :

STRUCTURES	Active Width (μm)	Tunnel Window (μm^2)
#1	0.6	0.6x0.6
#2	0.8	0.6x0.6
#3	1	0.6x0.6
#4	1.2	0.6x0.6
#5	1	Active widthx0.6
#6	1	0.3x0.3
#7	1	0.4x0.4
#8	1	0.5x0.5

Table 1 : Summary of the different geometries of each structure of TEG C

TEG C

PAD	STRUCTURES	DESCRIPTION
1	#1 tunnel oxide area defined in LV oxide : 2949 μm^2	Cell gate
2	#1 LV oxide area : 4915 μm^2	Transistor gate
3	#1	Substrate
4		GND

5	#2 LV oxide area : 6553.6 μm^2	Transistor gate
6	#2 tunnel oxide area defined in LV oxide : 2949 μm^2	Cell gate
7	#2	Substrate
8		GND
9	#3 LV oxide area : 8192 μm^2	Transistor gate
10	#3 tunnel oxide area defined in LV oxide : 2949 μm^2	Cell gate
11	#3	Substrate
12		GND
13	#4 LV oxide area : 9830.4 μm^2	Transistor gate
14	#4 tunnel oxide area defined in LV oxide : 2949 μm^2	Cell gate
15	#4	Substrate
16		GND
17	#5 tunnel oxide area defined in LV oxide : 4915.2 μm^2	Cell gate
18	#5 LV oxide area : 4915 μm^2	Transistor gate
19	#5	Substrate
20		GND
21	#6 tunnel oxide area defined in LV oxide : 737 μm^2	Cell gate
22	#6 tunnel oxide area : 8192 μm^2	Transistor gate
23	#6	Substrate
24		GND
25	#7 tunnel oxide area defined in LV oxide : 1310 μm^2	Cell gate
26	#7 LV oxide area : 8192 μm^2	Transistor gate
27	#7	Substrate
28		GND
29	#8 tunnel oxide area defined in LV oxide : 2048 μm^2	Cell gate
30	#8 LV oxide area : 8192 μm^2	Transistor gate
31	#8	Substrate
32		GND

Part 3)

This document is an updated description of the test structures inserted in the *ESSAII* module dedicated to parasitic transistors characterization.

TEG1: reachthrough HV parasitic transistors with varying capa implant/capa implant distance
(d). No contact to substrate.

Pad 27: $d=2.5\mu\text{m}$

Pad 28: $d=2\mu\text{m}$

Pad 29: $d=1.75\mu\text{m}$

Pad 30: $d=1.5\mu\text{m}$

Pad 31: $d=1.25\mu\text{m}$

Pad 32: $d=1\mu\text{m}$

TEG5: interdigitated HV parasitic transistors with varying capa implant/capa implant distance
(d). No contact to substrate. Source contact= Pad 27 TEG6.

Pad 27: GATE

Pad 28: $d=2.5\mu\text{m}$

Pad 29: $d=2\mu\text{m}$

Pad 30: $d=1.75\mu\text{m}$

Pad 31: $d=1.5\mu\text{m}$

Pad 32: $d=1.25\mu\text{m}$

Cross Kelvin Resistors and Van der Pauw structures:

It must be noted that for these structures the masks 735a and 745a are wrong (n+ contacts implant instead of p+ contact implant).

TEG12: Cross Kelvin Resistor on n+ diffusion (HV nat); $W(AA)=1.2\mu\text{m}$

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

TEG13: Cross Kelvin Resistor on n- diffusion (HV nat); $W(AA)=1.2\mu\text{m}$

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

TEG14: Cross Kelvin Resistor on n- diffusion (HV nat); 1• AA n+, 1• AA n-;
 $W(AA)=1.2\mu\text{m}$

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

TEG15: Van der Pauw structure for n+ sheet resistance measurement

TEG16: Van der Pauw structure for n- sheet resistance measurement

TEG17: Van der Pauw structure for n- sheet resistance measurement (1• AA n+, 1• AA n-)

TEG18: Cross Kelvin Resistor on p+ diffusion (HV nat); W(AA)=1.2μm

Pad 28: N-well contact

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

TEG19: Cross Kelvin Resistor on p- diffusion (HV nat); W(AA)=1.2μm

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

TEG20: Cross Kelvin Resistor on p- diffusion (HV nat); 1• AA p+, 1• AA p-;
W(AA)=1.2μm

Pad 29: M1

Pad 30: AA1

Pad 30: AA2

Pad 30: M2

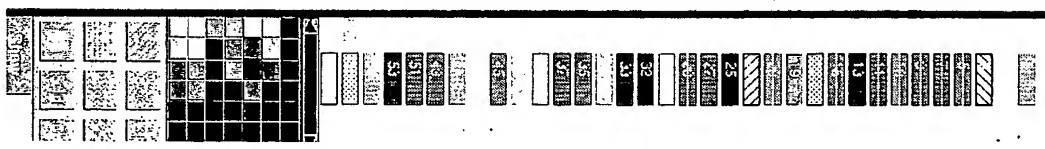
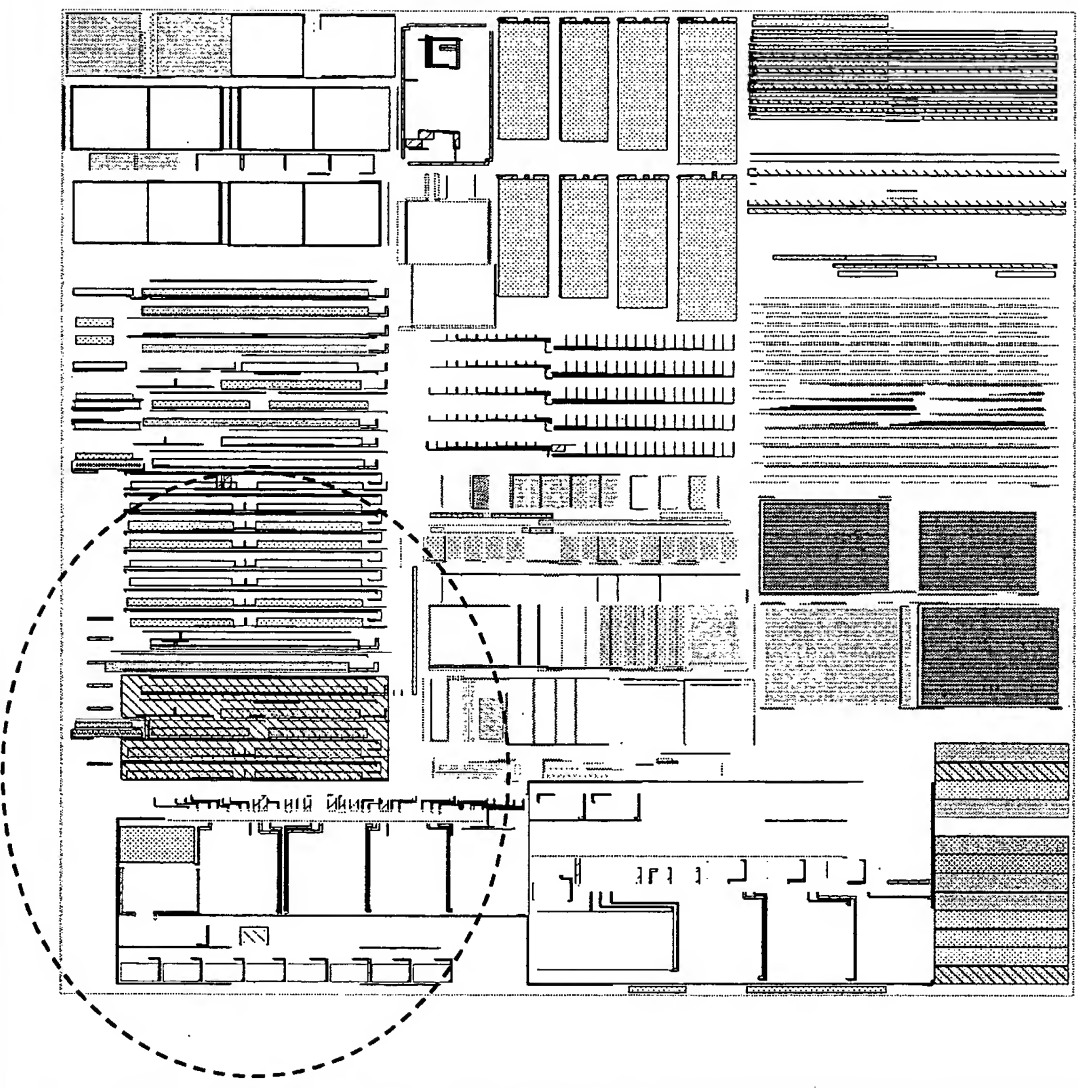
TEG21: Van der Pauw structure for p+ sheet resistance measurement

TEG22: Van der Pauw structure for p- sheet resistance measurement

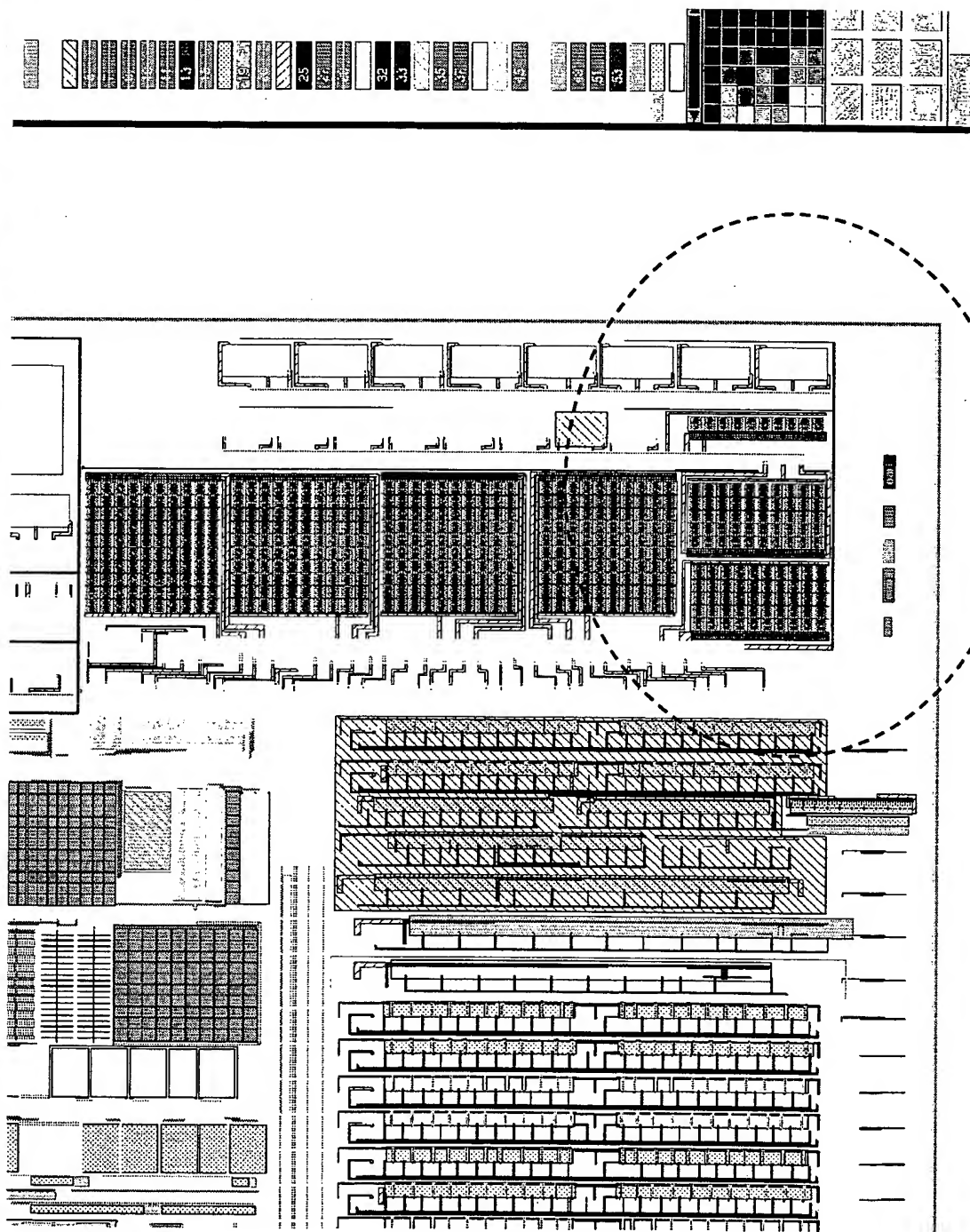
TEG25: Van der Pauw structure for p- sheet resistance measurement (1• AA p+, 1• AA p-)

APPENDIX ' 3

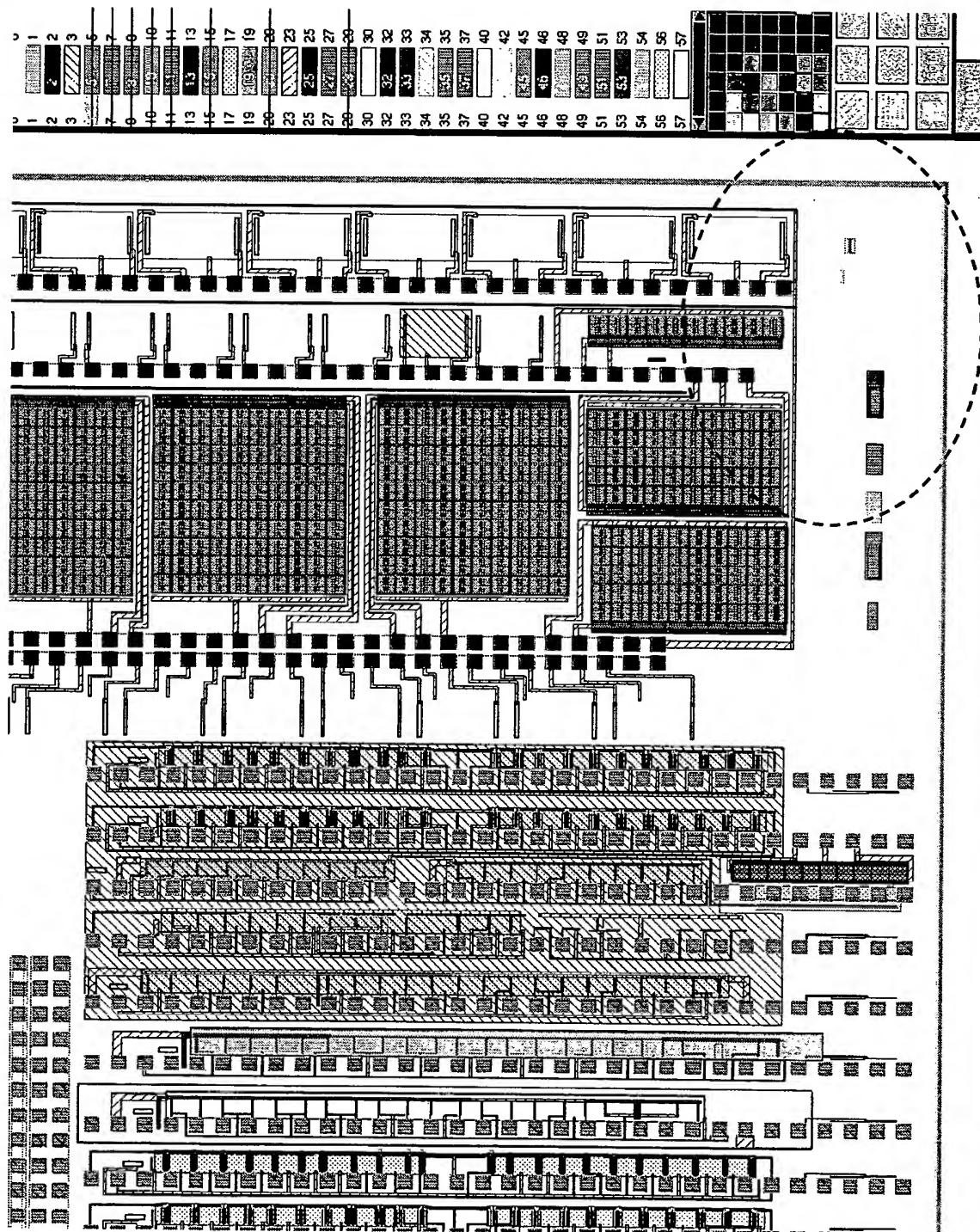
ZZ33 MASK SET: FULL LAYOUT



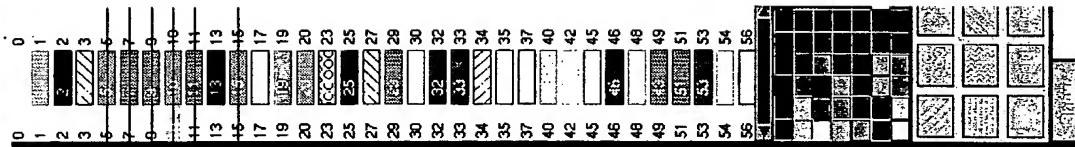
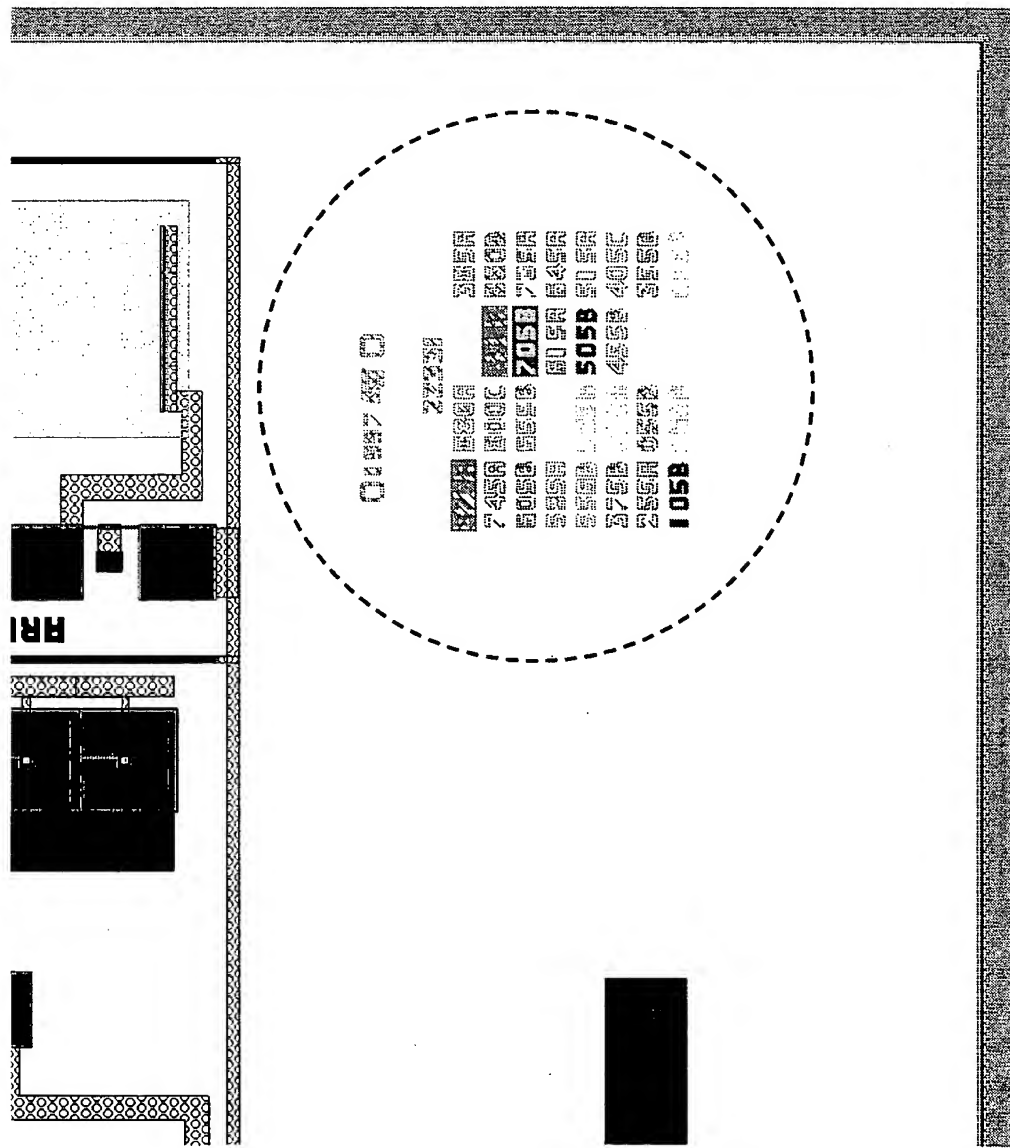
ZZ33: BOTTOM-RIGHT CORNER



ZZ33: BOTTOM-RIGHT CORNER



ZZ33: BOTTOM-RIGHT CORNER MASK NAMES, LOGO & YEAR

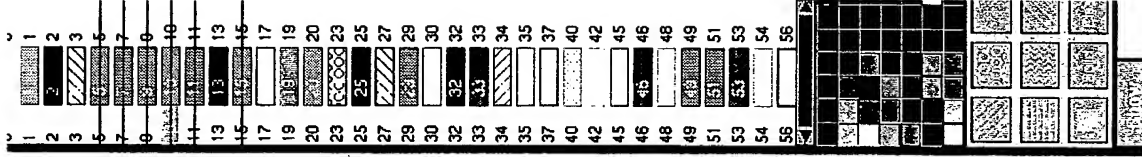


2233: MASK NAIVES, LOGO & YEAR

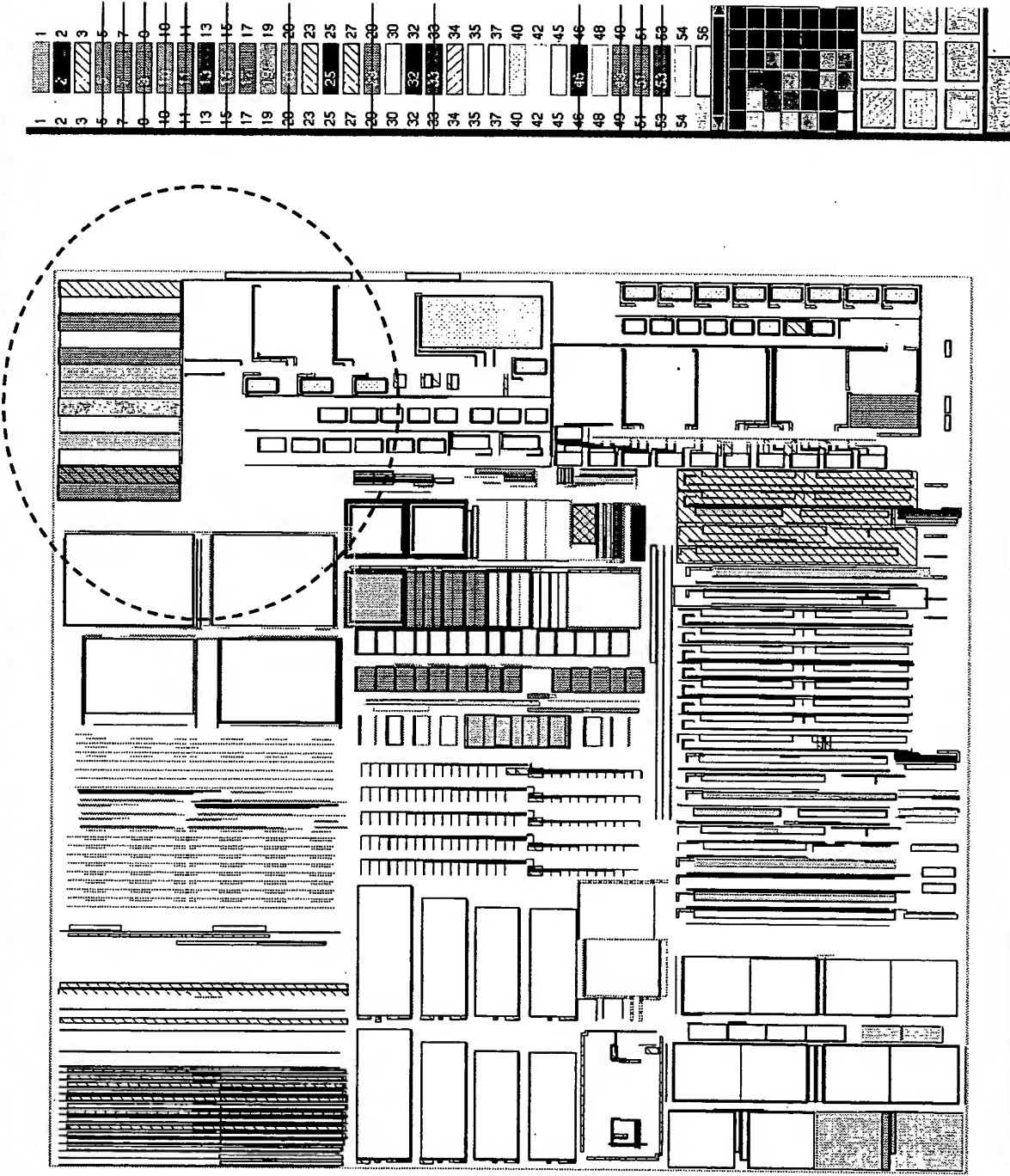
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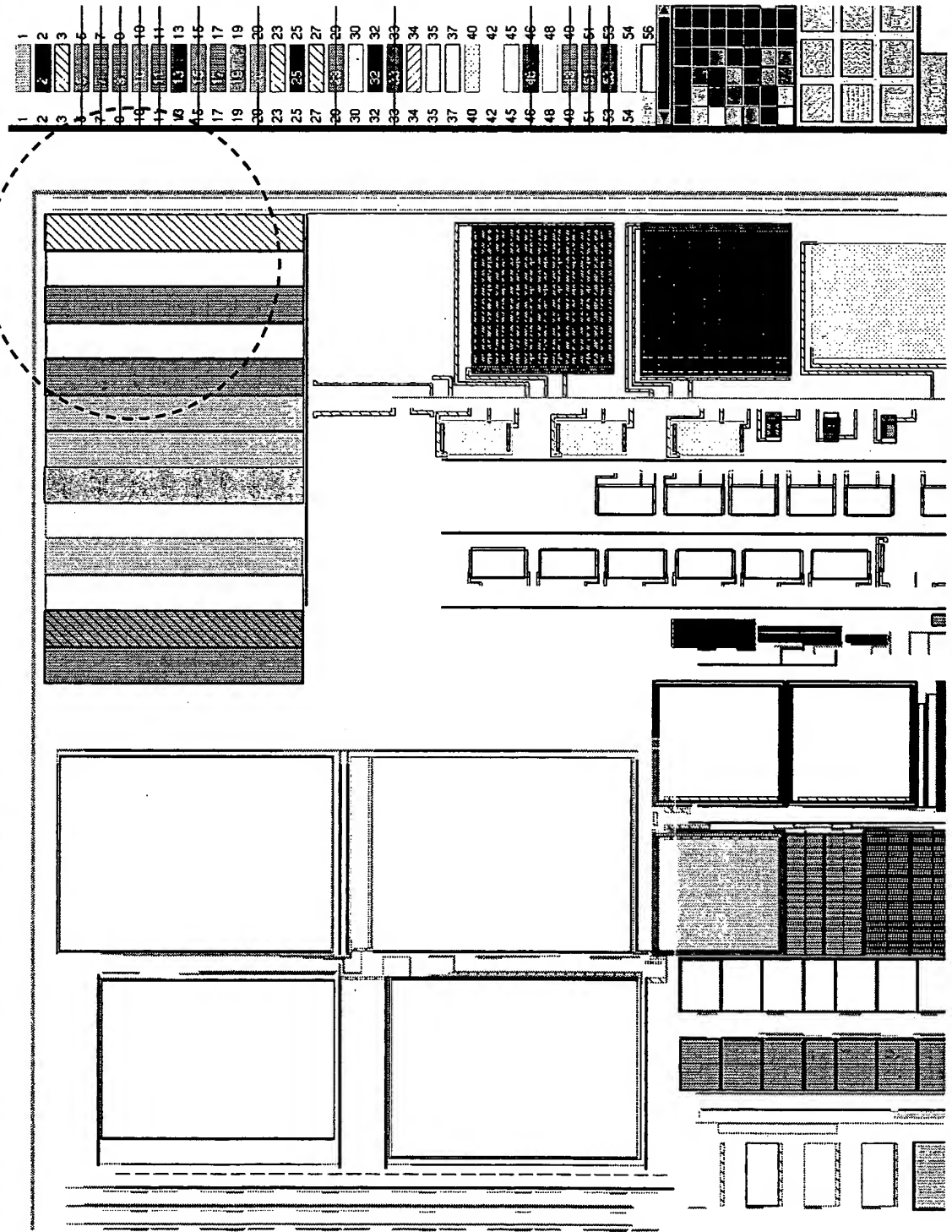
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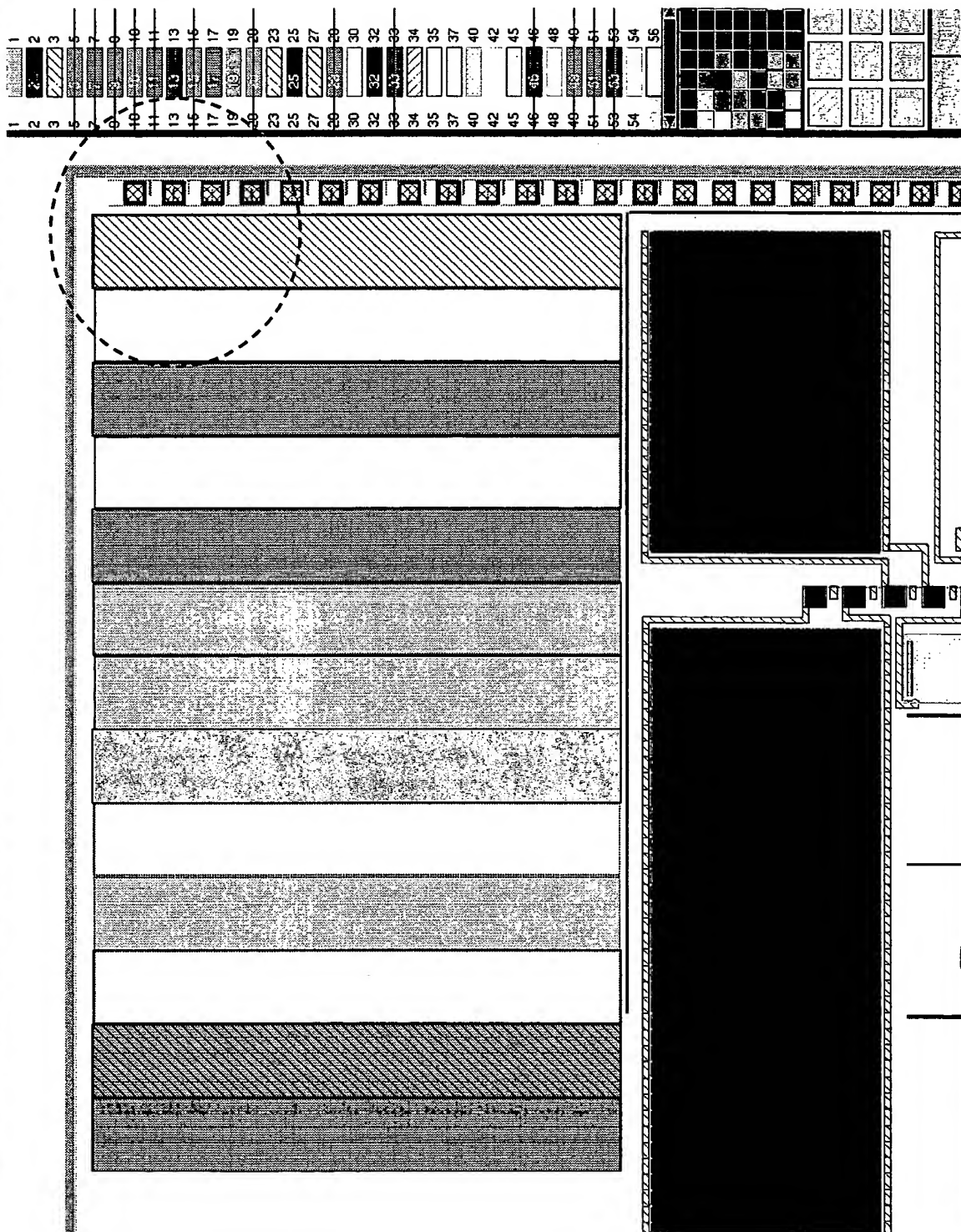
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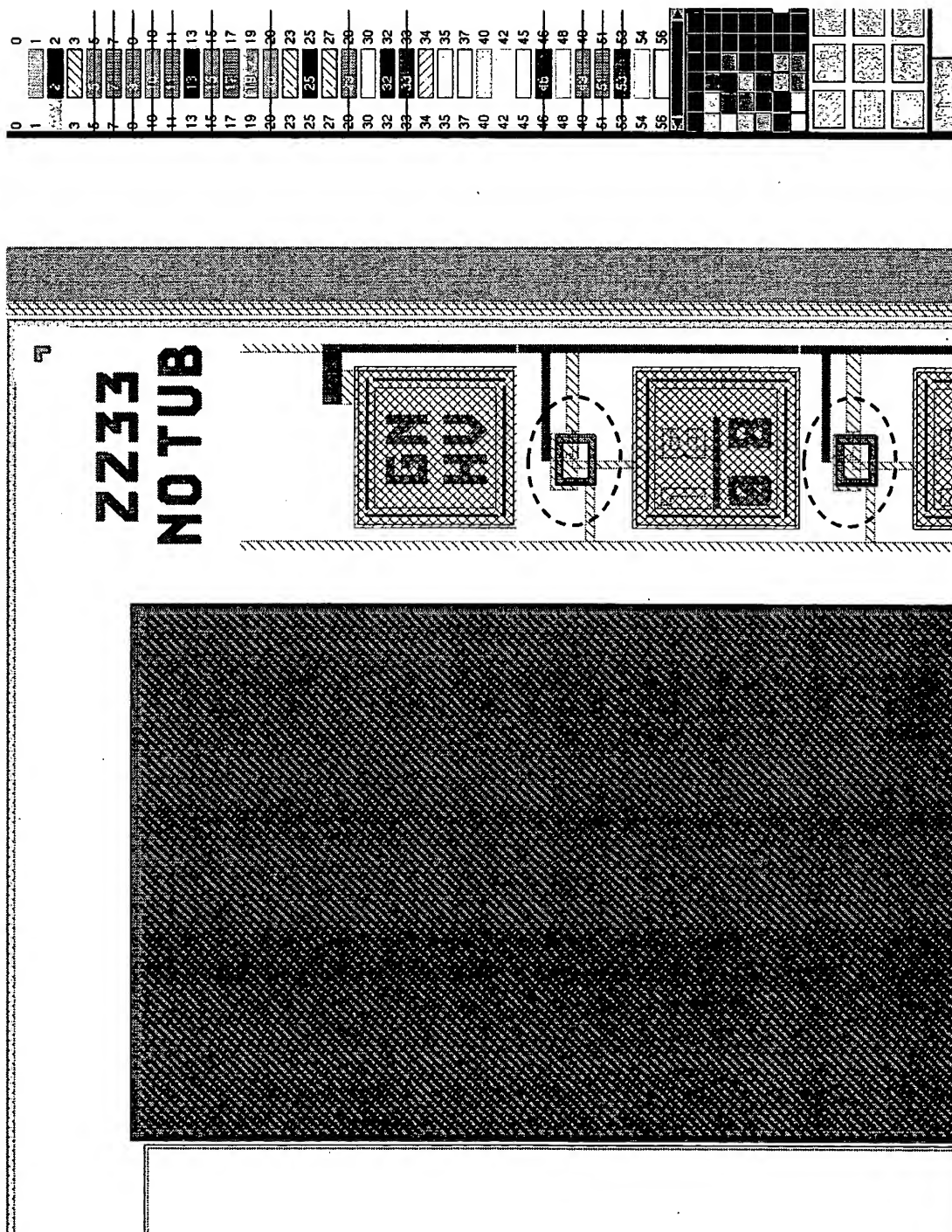
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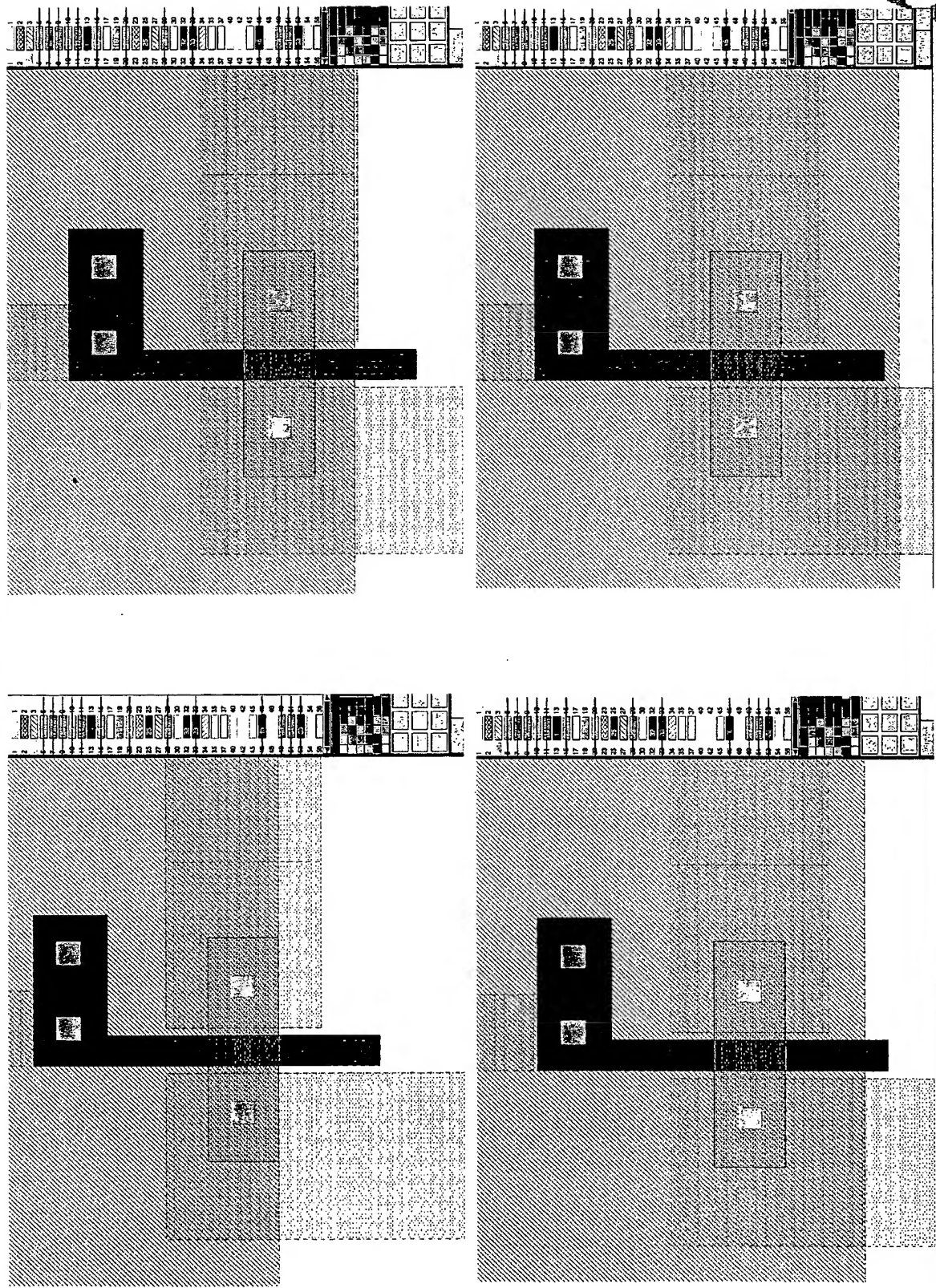
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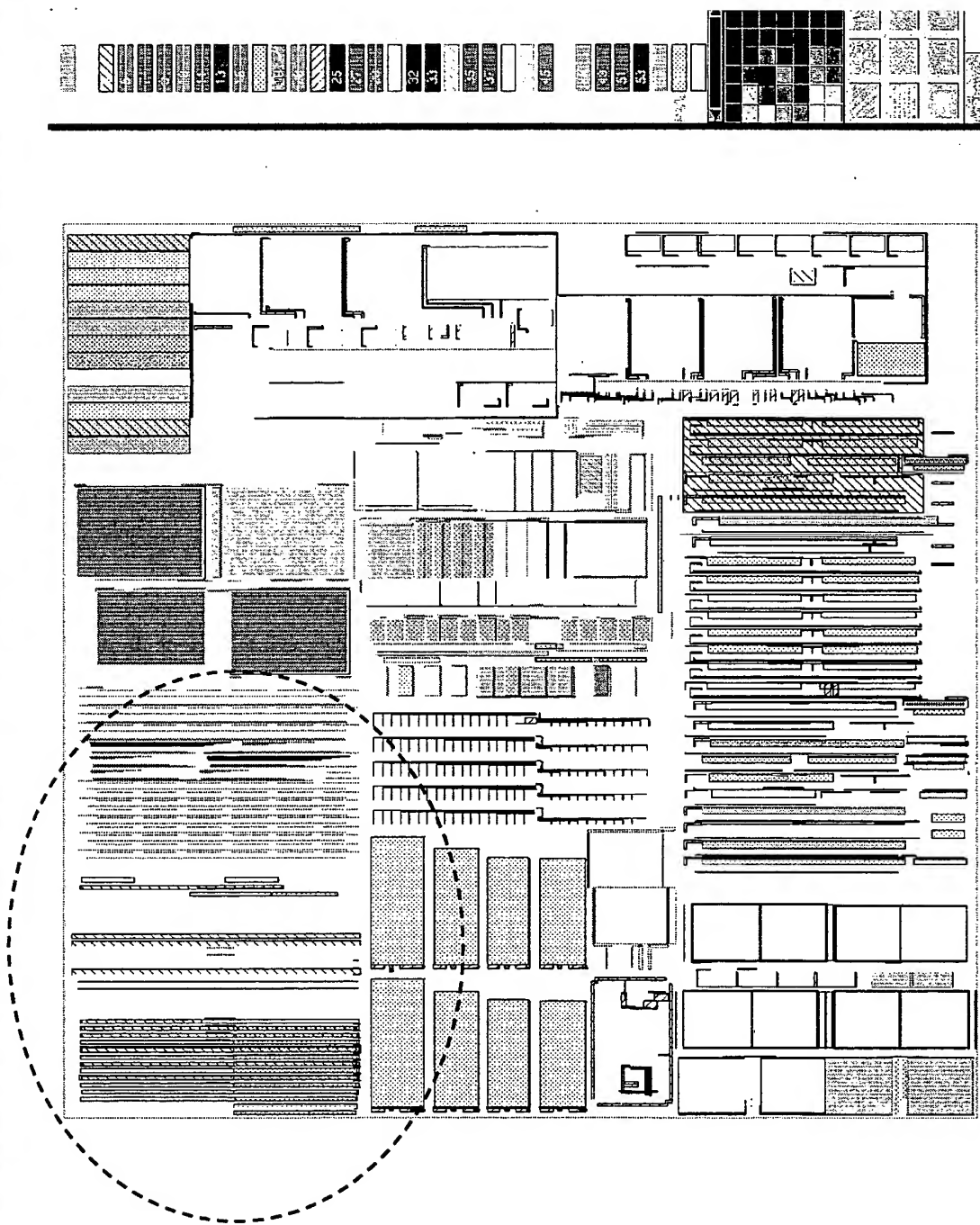
ZZ33: TEG WITH NoTub-Active (055-105) SPACING VARIATIONS



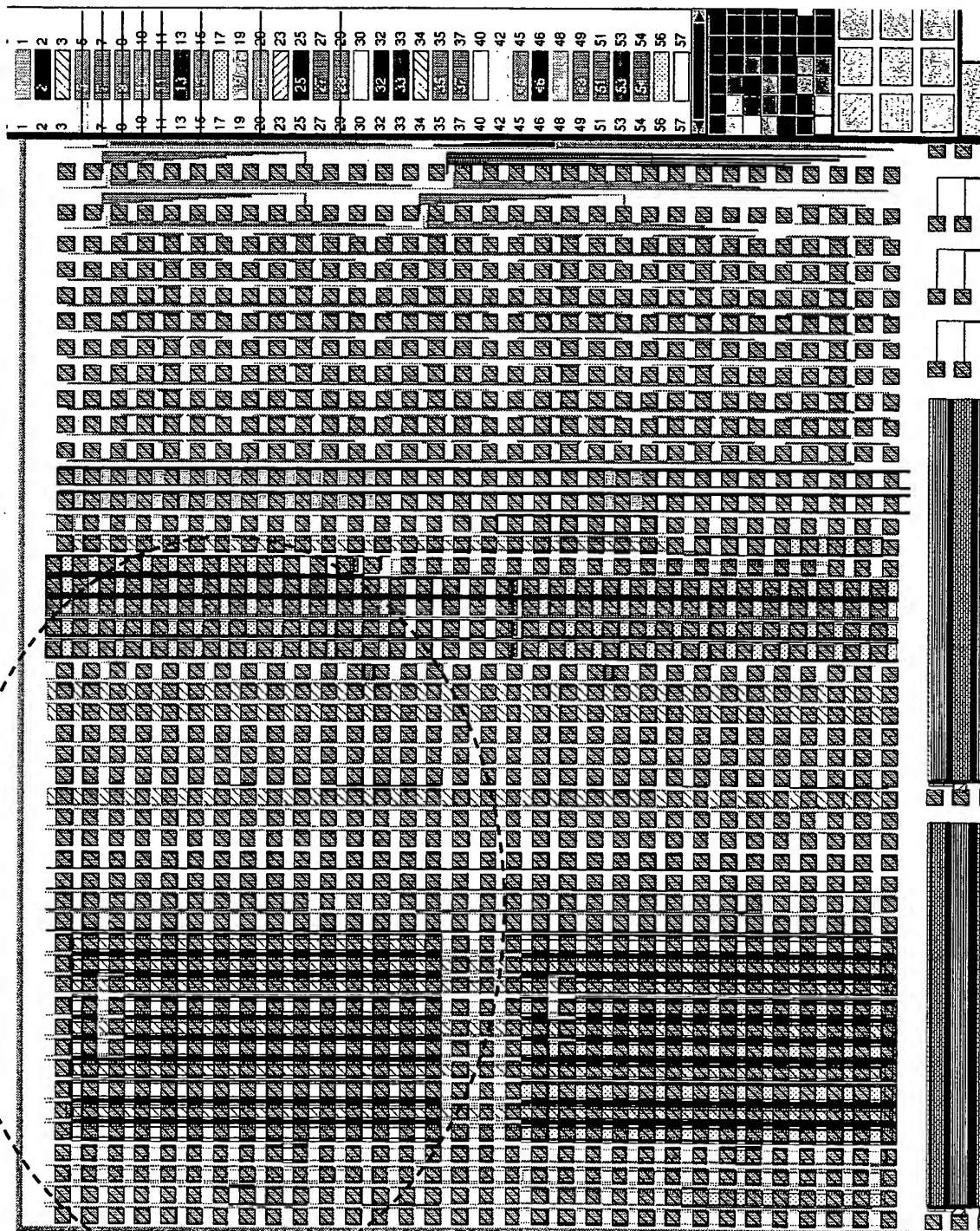
SPACING VARIATIONS (055-105 OVERLAP)



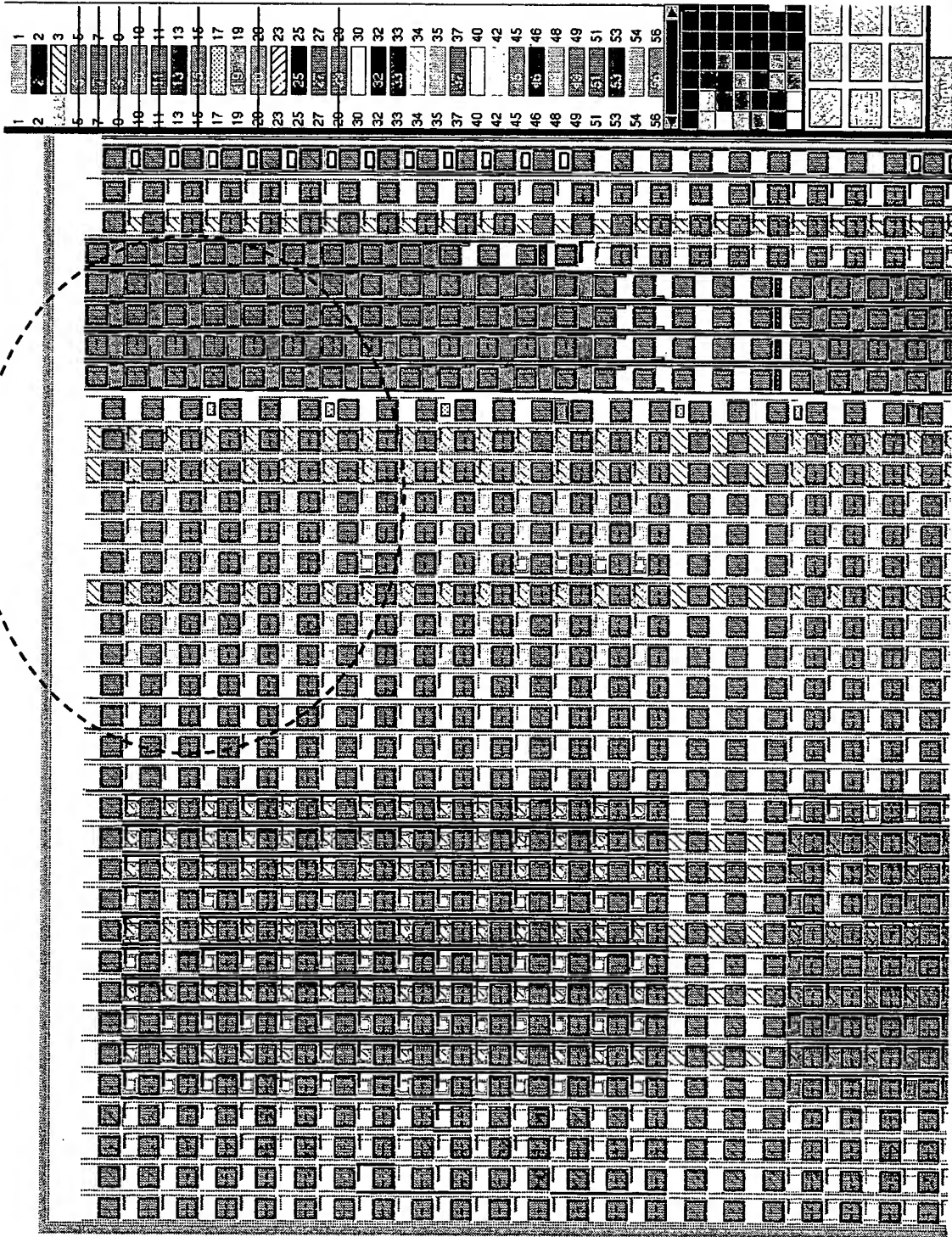
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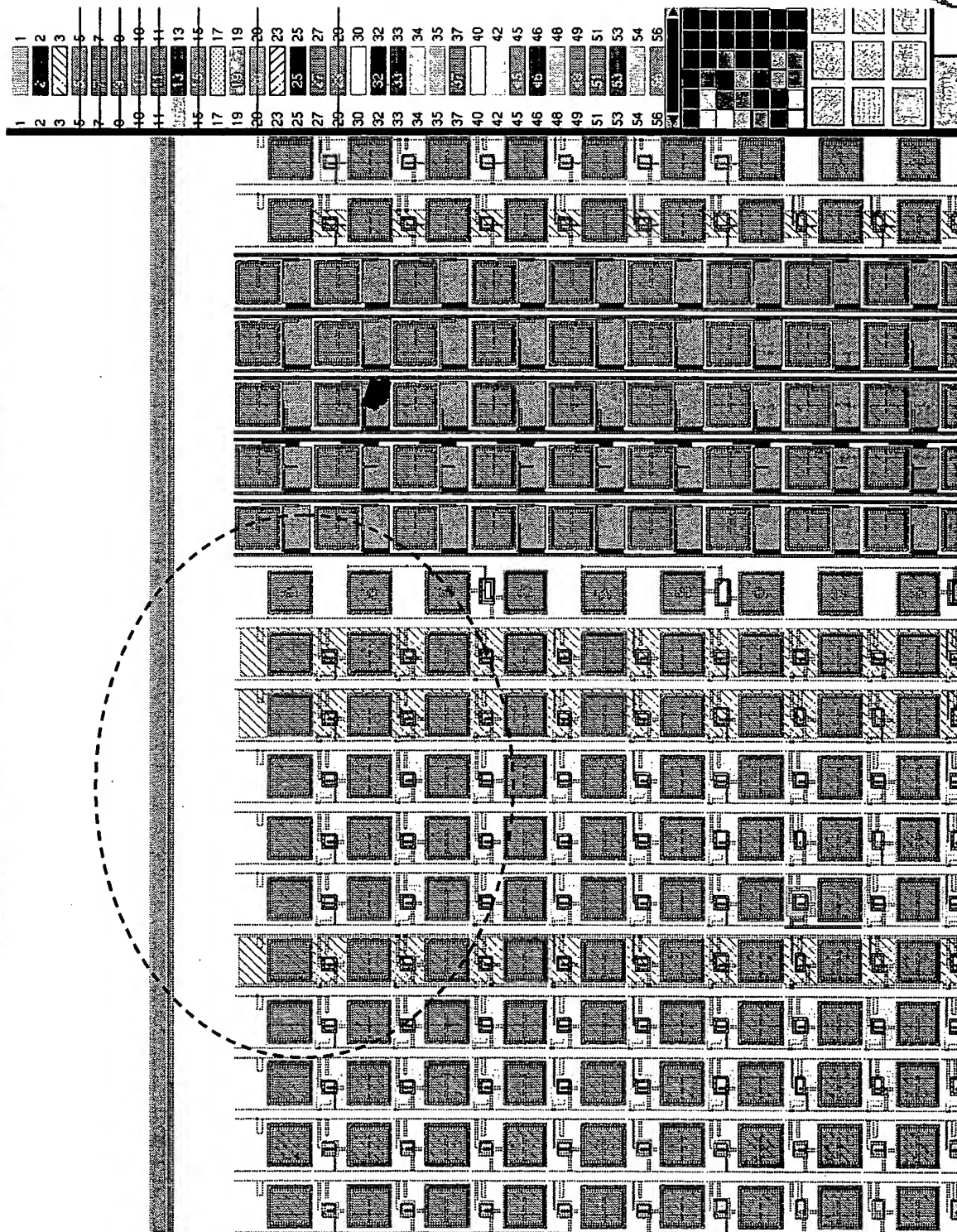
ZZ33: TOP-LEFT CORNER



ZZ33: TOP-LEFT CORNER

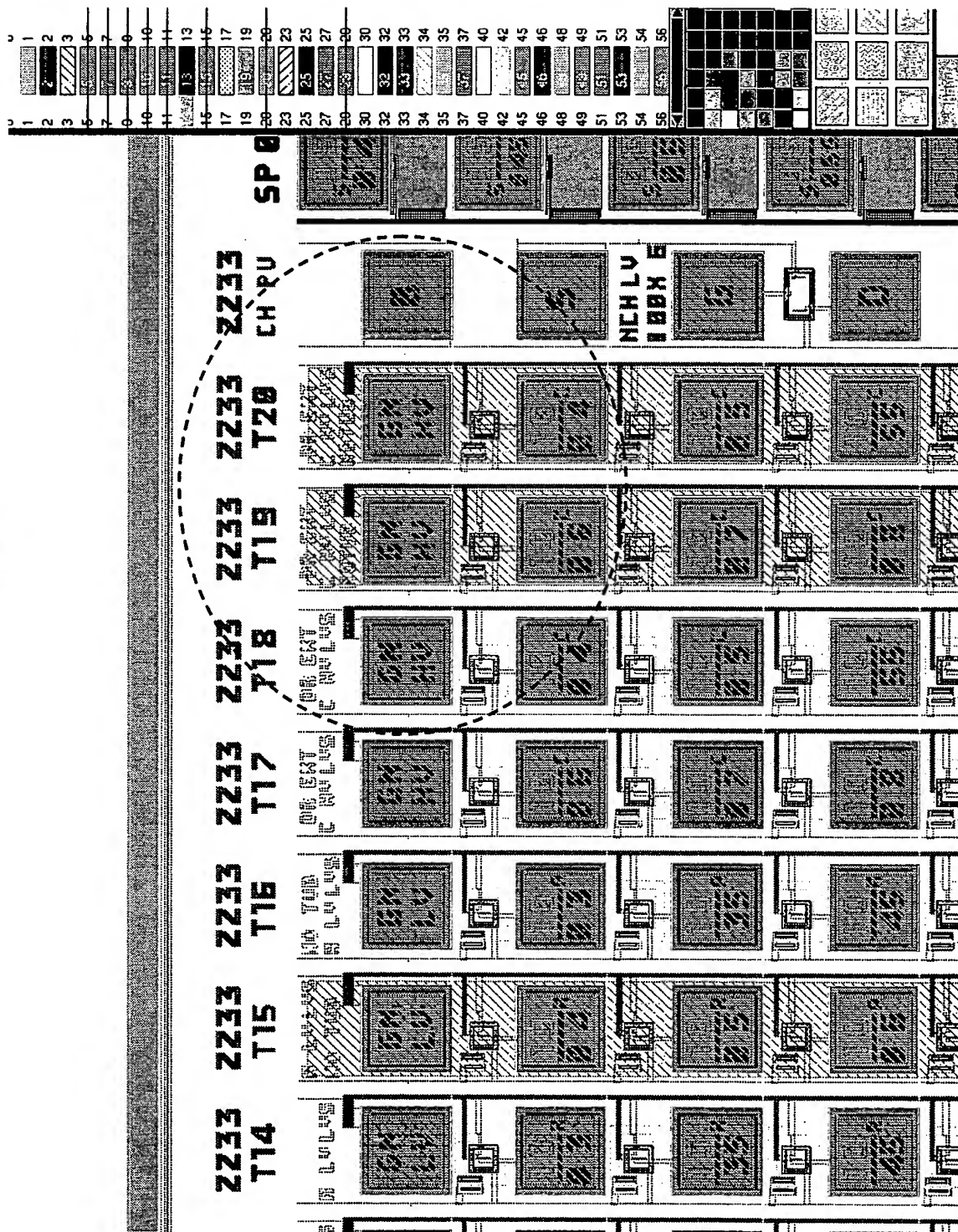


ZZ33: TOP-CENTER

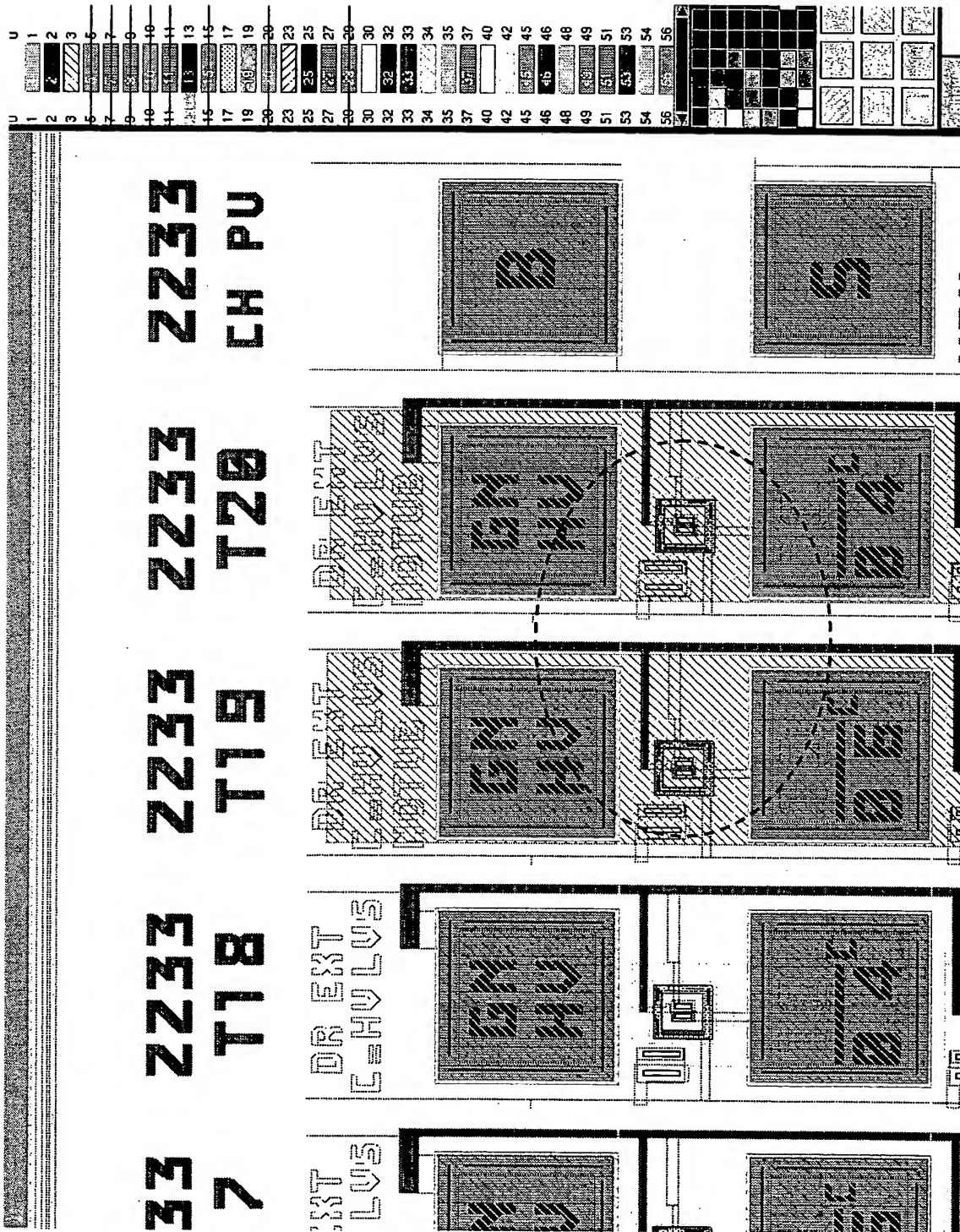


2233 TOP-CEN I ER: I EUS 15, 19 &

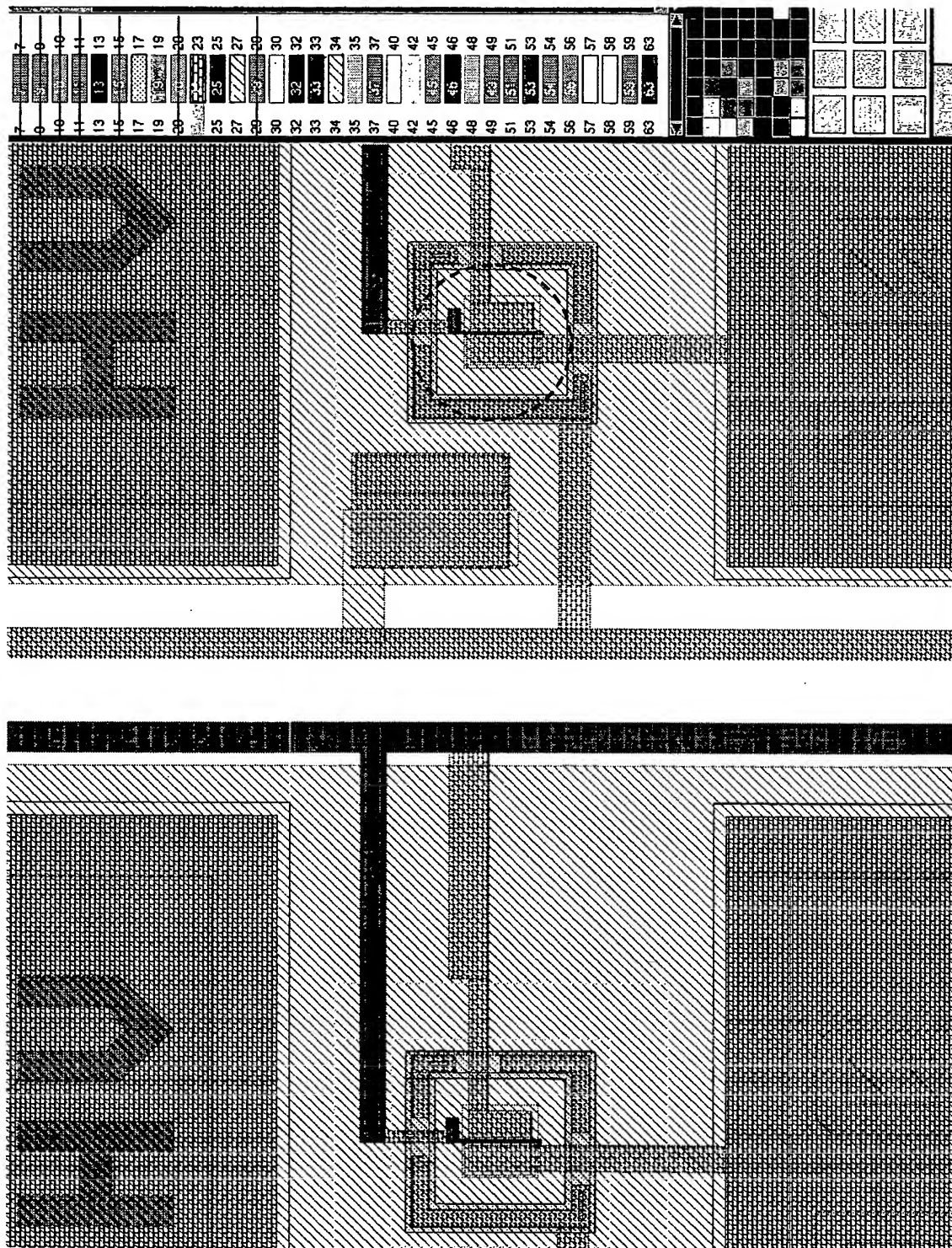
20



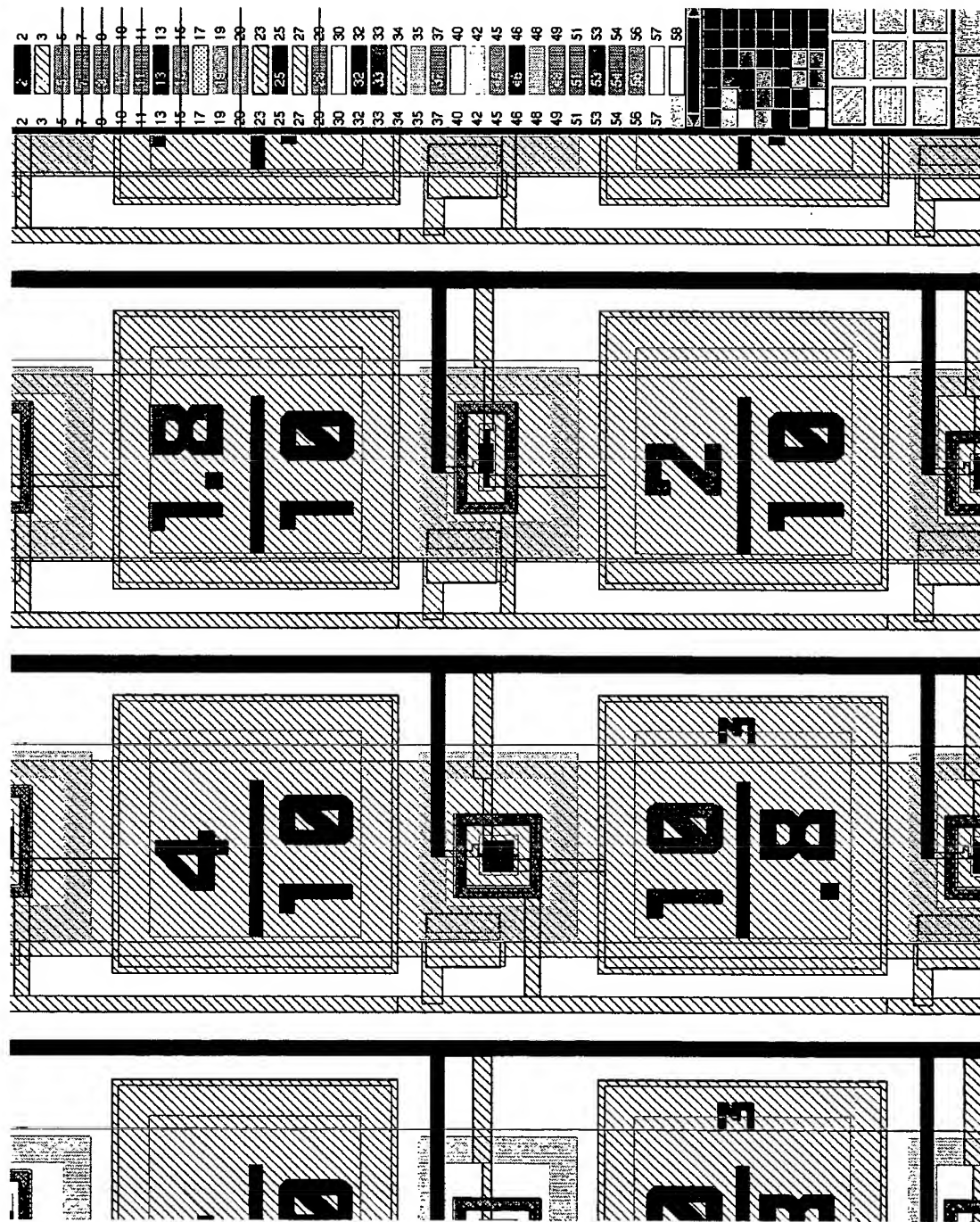
ZZ33 TOP: TEGS 19 & 20



ZZ33: TEGs 19 & 20, PADS 1 & 2

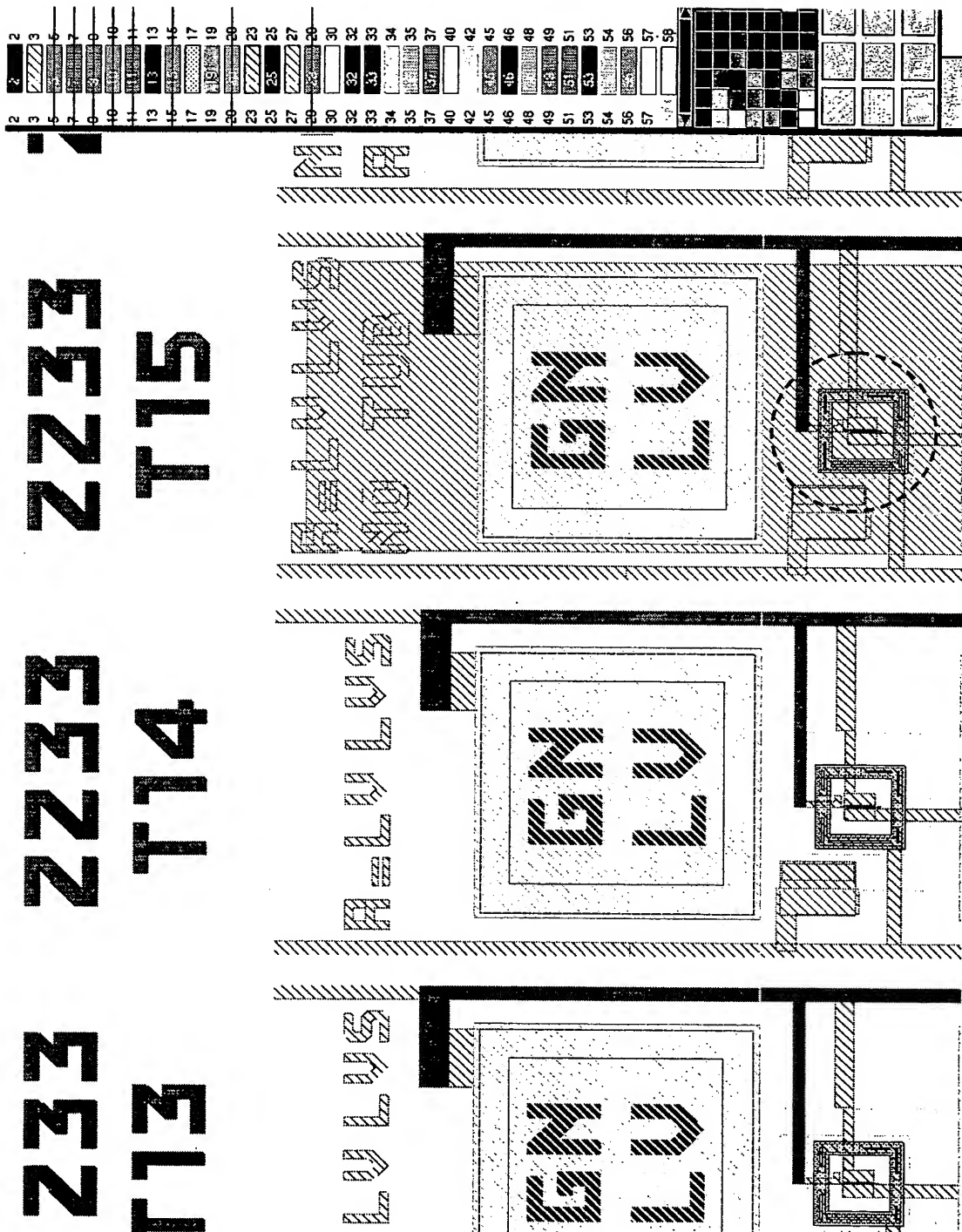


ZZ33 TEGs 12 and 25, PADs 26 and 27 NoTub trans. with different geometries

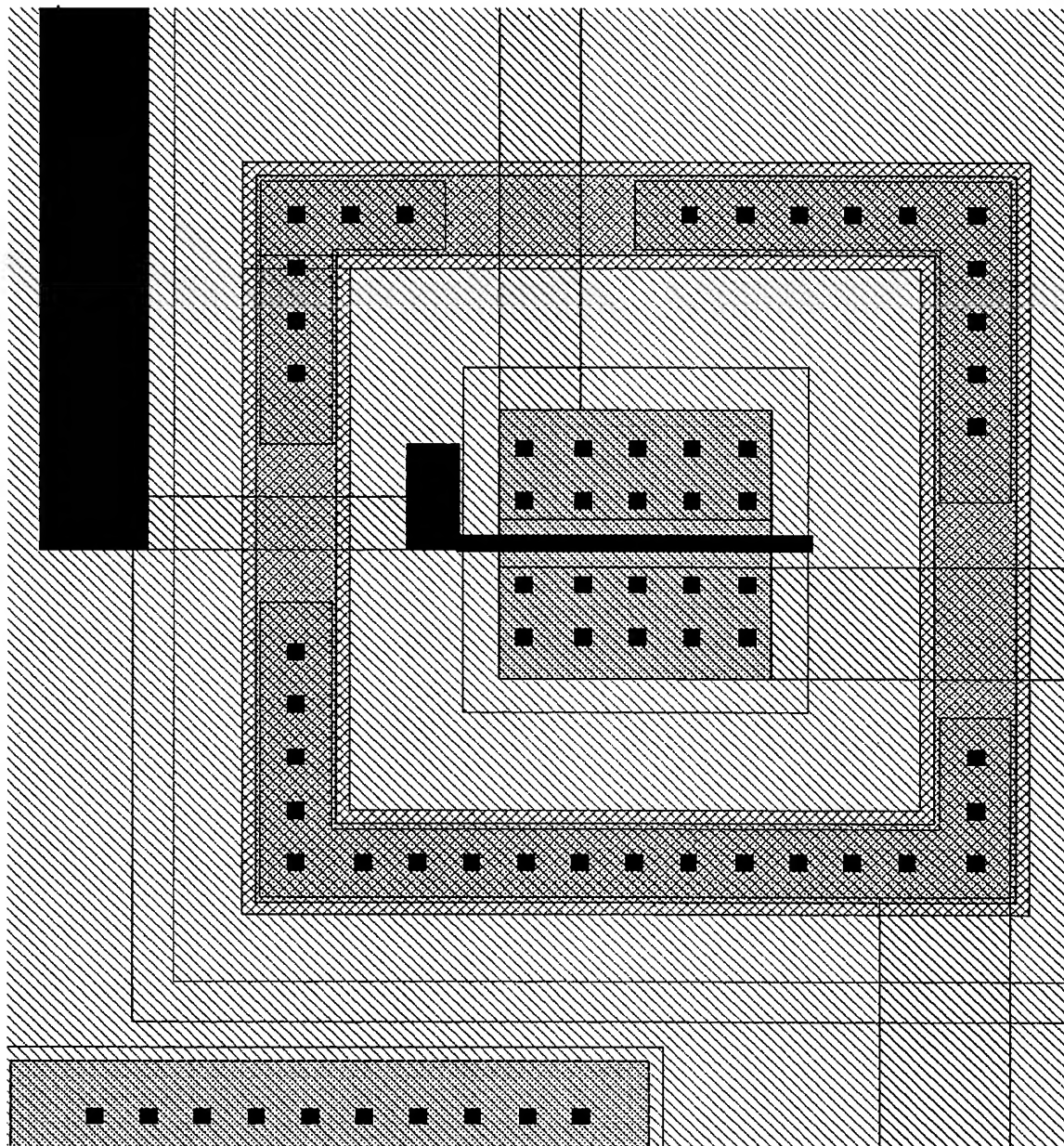


ZZ33 IUP: LEGS (13, 14) & 15, PADS 1

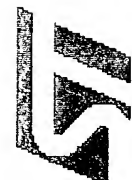
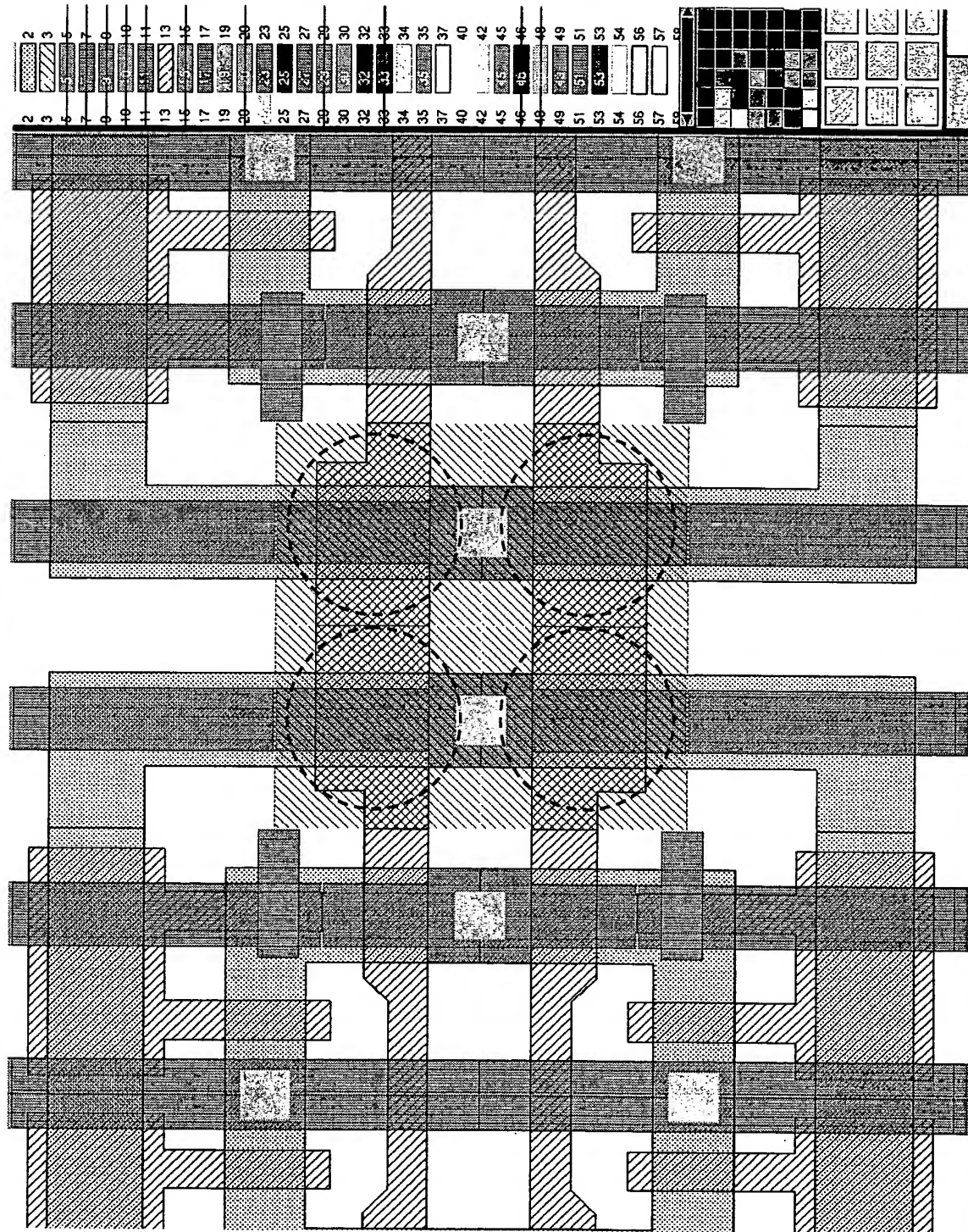
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T73 T74 T75



LV NO IUD TRANSISTOR



2233: NO I UD I R. in singieroy CELL



APPENDIX ' 4



COMPANY RESTRICTED

I.C. 210.1047.97

Agrate, December 11th, 1997

From: P.Zuliani

To: F.Pio
B.Vajana
N.Zatelli
G.Dalla Libera
C.Cremonesi
M.T.Sala
M.Patelmo
M.Tormen
O.Pizzuto (Rousset)
J.M.Mirabel (Rousset)
F.Tailliet (Rousset)
M.Lisart (Rousset)
S.Wuidart (Rousset)
N.Demange (Catania)
A.Marmioli
G.Valentini

CC: L.Baldi
G.Crisenza
L.Sourgen (Rousset)
J.Lopez (Rousset)
M.Gaibotti (Catania)

OBJECT: *Electrical characterization of CMOS F6X active transistors
from first lot out (SP process option)*

Approved by: L.Baldi

INTRODUCTION

In this report the electrical characterization of the first lot processed with CMOS F6X SP flow and the dedicated T.P.ZZ33 set of masks will be summarized. The results obtained from the parametric test T84 have been verified at bench on some splits. A complete electrical characterization of transistors has been performed on the trial which has revealed not far from the target values of CMOS F6X 0.5 μ m technology (SmartCards/ EEPROM standalone memories dedicated). This work has been realized on the first lot available for the debugging of the new Test Pattern.

PROCESS DESCRIPTION

The main process steps of CMOS F6X SP flow affecting transistors performance can be summarized in the following way. It must be pointed out that the full drain extension option has been adopted for HV transistors in order to support the high internal voltage (18V) needed to perform the electrical programming of EEPROM standalone memories. The indication of the implants needed for the different kind of transistors is also given. The no-tub option is meaningful only for HV transistors.

☐ *n-ch transistors implants*

		<i>nat</i>	<i>LVS</i>	<i>nat notub</i>	<i>LVS notub</i>
<i>P-iso mask (255)</i>					
<i>p-iso:</i>	B 3.5E12 cm ⁻² 180 keV	y	y	y	y
<i>P-tub mask (055)</i>					
<i>p-well:</i>	B 1.0E13 cm ⁻² 700 keV	y	y	n	n
<i>1 (HV&LV) LVS:</i>	B 1.5E12 cm ⁻² 50 keV	y	y	n	n
<i>LVS mask (355)</i>					
<i>2 (HV&LV) LVS:</i>	B 4.2E12 cm ⁻² 50 keV	n	y	n	y
<i>(HV&LV) anti-PT:</i>	B 4.0E12 cm ⁻² 140 keV	n	y	n	y
<i>n⁻ implant mask (615)</i>					
<i>(HV&LV) n⁻ LDD:</i>	P 4x(0.5E13) cm ⁻² 70 keV	y	y	y	y
<i>n⁺ implant mask (605)</i>					
<i>S&D n⁰ (LV):</i>	P 4x(5.0E13) cm ⁻² 80 keV	y	y	-	-
<i>S&D n⁺ (LV):</i>	As 4.0E15 cm ⁻² 35 keV	y	y	-	-
<i>n⁺ contact implant mask (735)</i>					
<i>n⁺ contact:</i>	As 1.0E15 cm ⁻² 60 keV	y	y	y	y

☐ *p-ch transistors implants*

			<i>nat</i>	<i>LVS</i>
<i>N-well mask (015)</i>				
<i>n-well:</i>	P31	1.0E13 cm ⁻² 1200 keV	y	y
<i>HV&LV n-iso:</i>	P31	2.0E12 cm ⁻² 500 keV	y	y
<i>1 LVS (HV&LV):</i>	B11	1.7E12 cm ⁻² 25 keV	y	y
<i>1 aPT (HV&LV):</i>	P31	1.0E12 cm ⁻² 180 keV	y	y
<i>LVS p-ch mask (305)</i>				
<i>2 LVS (HV&LV):</i>	B11	2.0E12 cm ⁻² 25 keV	n	y
<i>2 aPT (HV&LV):</i>	P31	2.0E12 cm ⁻² 180 keV	n	y
<i>p⁻ implant mask (645)</i>				
<i>p⁻ LDD:</i>	BF2	1.0E13 cm ⁻² 100 keV	y	y
<i>p⁺ implant mask (655)</i>				
<i>S&D p⁺ (LV):</i>	BF2	3.0E15 cm ⁻² 40 keV	y	y
<i>p⁺ contact implant mask (745)</i>				
<i>p⁺ contact:</i>	BF2	6.0E14 cm ⁻² 40 keV	y	y

☐ *Dopant activation*

The dopant activation has been performed by means of the following thermal treatments:

- 1st source and drain reoxidation at 900°C, 45 min O₂ (final thickness 170Å)
- 2nd source and drain reoxidation at 900°C, 20 min O₂ (final thickness 100Å)
- a first RTP (BPSG reflow) at 1050 C, 30 sec N₂
- a second RTP (contacts) at 810 C, 30 sec N₂

☐ *Oxides*

- nominal HV oxide thickness 180Å, target final value 220Å
- nominal LV oxide thickness 100Å, target final value 120Å
- nominal tunnel oxide thickness 60Å

EXPERIMENTAL

Measurements were performed on lot V729501 and results have been substantially confirmed by two other Single-Poly lots then available (V731895 and V733286). The transistor dimensions reported here on are the nominal one ($L=L_{nom}$, $W=W_{nom}$). The following relation holds between nominal and on mask dimension for the ZZ33 set of masks:

$$\begin{aligned} L_{mask} &= L_{nom} \\ W_{mask} &= W_{nom} + 0.5\mu m \end{aligned}$$

(O.V.=0.25 μ m on the Active Area).

Measurements were mainly performed using Labview programs.

ELECTRICAL PARAMETERS

In the following tables the electrical parameters (measured at T84) of the different transistors available on the T.P. ZZ33 are collected and the effect of the different implant trials pointed out. The trials performed mainly concern p-iso and anti-punchthrough implant for n-channel transistors (the last one effective only on the "LVS" ones), 1st and 2nd anti-punchthrough and p⁻ LDD implant for p-channel transistors. Threshold voltages, breakdown voltages (measured at 10nA) and saturation current (at $V_d=V_g=5V$) are reported for square and typical transistors.

Table 1. n-ch HV LVS

<i>p-iso</i>	<i>a-PT</i>	V_t (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
		10/10	10/0.8	10/10	10/0.8	10/10	10/0.8
B 3.5e12 cm ⁻² 180 keV	no implant	1.75	1.78	16.1	16.1	16	100
"	B 2.0e12 cm ⁻² 140 keV	1.80	1.80	13.7	13.7	16	93
"	B 4.0e12 cm ⁻² 140 keV	1.80	-	12.4	12.4	15	85
no implant	no implant	1.7	1.7	19.9	19.9	17	110
"	B 2.0e12 cm ⁻² 140 keV	1.75	-	18.4	18.4	16	100
"	B 4.0e12 cm ⁻² 140 keV	1.8	-	14.8	14.8	15	900

Table 2. n-ch native HV

<i>p-iso</i>	<i>a-PT</i>	$V_t (V)$		$BV (V)$		$I_{dsat} (\mu A/\mu m)$	
		10/10	10/0.8	10/10	10/0.8	10/10	10/0.8
B 3.5e12 cm ⁻² 180 keV		0.3	0.33	15.6	15.1	36	20
no implant		0.76	0.71	18.2	17.8	42	240

Table 3. n-ch HV LVS no-tub

<i>p-iso</i>	<i>a-PT</i>	$V_t (V)$		$BV (V)$		$I_{dsat} (\mu A/\mu m)$	
		10/10	10/0.8	10/10	10/0.8	10/10	10/0.8
B 3.5e12 cm ⁻² 180 keV	no implant	1.5	1.49	17.4	17.4	20	100
"	B 2.0e12 cm ⁻² 140 keV	1.6	1.53	14.2	14	20	110
"	B 4.0e12 cm ⁻² 140 keV	1.56	-	13	13	19	130
no implant	no implant	1.43	1.47	18	18.1	22	140
"	B 2.0e12 cm ⁻² 140 keV	1.5	-	19.5	-	21	120
"	B 4.0e12 cm ⁻² 140 keV	1.6	-	16	16.1	20	110

Table 4. n-ch HV native no-tub

<i>p-iso</i>	<i>a-PT</i>	$V_t (V)$		$BV (V)$		$I_{dsat} (\mu A/\mu m)$	
		10/10	10/0.8	10/10	10/0.8	10/10	10/0.8
B 3.5e12 cm ⁻² 180 keV		0.30	0.24	18.3	19.7	53	260
no implant		-	-	19.4	-	78	360

Table 5. n-ch LV LVS

<i>p</i> -iso	<i>a</i> -PT	V_i (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
		10/10	10/0.6	10/10	10/0.6	10/10	10/0.6
B 3.5e12 cm ⁻² 180 keV	no implant	0.82	0.8	16.8	12	58	480
"	B 2.0e12 cm ⁻² 140 keV	0.86	0.84	14.1	11.1	55	460
"	B 4.0e12 cm ⁻² 140 keV	0.86	0.84	14.1	11.1	55	460
no implant	no implant	0.81	0.78	17	12.3	60	490
"	B 2.0e12 cm ⁻² 140 keV	0.83	0.81	18.6	12	58	480
"	B 4.0e12 cm ⁻² 140 keV	0.86	0.84	15.6	11.8	55	460

Table 6. n-ch native LV

<i>p</i> -iso	<i>a</i> -PT	V_i (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
		10/10	10/1	10/10	10/1	10/10	10/1
B 3.5e12 cm ⁻² 180 keV		0.32	0.32	13.1	12.3	100	510
no implant		0.27	0.25	13.4	10	110	560

Table 7. p-ch HV LVS

1 <i>a</i> -PT	2 <i>a</i> -PT	<i>p</i> -LDD	V_i (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
			10/10	10/1	10/10	10/1	10/10	10/1
P 1.0e12 cm ⁻² 180 keV	P 2.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.96	-0.96	-13.8	-13.8	12	100
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-0.96	-0.96	-13.8	-13.8	11	68
no implant	no implant	BF ₂ 5.0e13 cm ⁻² 100keV	-	-	-	-	23	180
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-	-	-	-	24	130
"	P 2.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.30	-0.30	-13.8	-	17	140
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-0.30	-0.30	-16.5	-	16	92
"	P 3.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.98	-	-13.8	-13.8	11	100
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-0.96	-0.98	-17.9	-17.9	11	68

Table 8. p-ch native HV

1 a-PT	2 a-PT	p LDD	V_t (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
			10/10	10/1	10/10	10/1	10/10	10/1
P 1.0e12 cm ⁻² 180 keV		BF ₂ 5.0e13 cm ⁻² 100keV	-0.95	-0.95	-14	-14	12.5	120
		BF ₂ 1.0e13 cm ⁻² 100keV	-0.95	-0.95	-18.5	-18.5	12	80
no implant		BF ₂ 5.0e13 cm ⁻² 100keV	-0.96	-0.92	-14.1	-14.1	20	160
"		BF ₂ 1.0e13 cm ⁻² 100keV	-	-	-	-	20	110

Table 9. p-ch LV LVS

1 a-PT	2 a-PT	p LDD	V_t (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
			10/10	10/0.6	10/10	10/0.6	10/10	10/0.6
P 1.0e12 cm ⁻² 180 keV	P 2.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.94	-	-11.2	-	22.5	380
		BF ₂ 1.0e13 cm ⁻² 100keV	-0.94	-0.88	-12.8	-12.7	22	250
no implant	no implant	BF ₂ 5.0e13 cm ⁻² 100keV	-	-	-	-	48	390
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-	-	-	-	55	300
"	P 2.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.62	-	-11.5	-	25	480
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-0.62	-0.52	-13.0	-	27	400
"	P 3.0e12 cm ⁻² 180 keV	BF ₂ 5.0e13 cm ⁻² 100keV	-0.94	-0.87	-12.7	-12.7	22	380
"	"	BF ₂ 1.0e13 cm ⁻² 100keV	-0.95	-0.87	-12.9	-12.8	22	363

Table 10. p-ch native LV

1 a-PT	2 a-PT	p LDD	V_t (V)		BV (V)		I_{dsat} ($\mu A/\mu m$)	
			10/10	10/0.6	10/10	10/0.6	10/10	10/0.6
P 1.0e12 cm ⁻² 180 keV		BF ₂ 5.0e13 cm ⁻² 100keV	-0.91	-0.91	-11.4	-	23	400
		BF ₂ 1.0e13 cm ⁻² 100keV	-0.92	-0.84	-13.2	-10.9	23	280
no implant		BF ₂ 5.0e13 cm ⁻² 100keV	-0.55	-0.55	-11.5	-	31	470
"		BF ₂ 1.0e13 cm ⁻² 100keV	-0.53	-0.45	-13.5	-	31	340

From the analysis of the different kind of transistors available on the Test Pattern and processed with F6X flow, it can be concluded that:

- ☐ the n-ch HV LVS transistors show an excessively high threshold voltage (1.8V)
- ☐ the n-ch native HV transistors, on the contrary, show reasonable threshold voltage both in the tub and no-tub options (approximately 0.85V and 0.3V) and breakdown voltages higher than 18V
- ☐ for the n-channel low voltage transistors both the LVS and native versions are acceptable (threshold voltages 0.9V and 0.3V respectively)
- ☐ no substantial difference can be found between threshold voltage of LVS and native p-channel transistors, both for high voltage and low voltage ones. For HV transistors breakdown voltages higher than 18V are observed in both cases.

From these considerations, the following transistors are found acceptable as obtained from F6X process flow:

- n-ch HV nat
- n-ch HV nat no-tub
- n-ch LV LVS
- n-ch LV nat

As far as p-channel transistors are considered, as it will be shown in the following, some marginality has been found on gate length of LV ones. For this reason the p-ch transistors considered to gain some degree of freedom in the design of their architecture will be:

- p-ch HV nat
- p-ch LV LVS ("LVS" 375 mask dedicated)

Further considerations on the effect of the different trials performed on this lot can be summarized as follows:

- the negative effect induced on breakdown voltages of n-channel transistors by increasing doses of anti-punchthrough implants is confirmed
- the major effect on the breakdown voltage of p-channel transistors is instead produced by the p⁺ LDD implant dose (the present standard has then been fixed as BF₂ 1e13 cm⁻² 100 keV)
- the 2nd LVS implant is not effective in reducing (in absolute value) the threshold voltage of p-channel transistors
- p-channel HV LVS transistors show electrical parameters similar to the native ones
- final oxide thickness on silicon:

$$HV=245\text{\AA}$$

$$LV=115\text{\AA}$$

The HV oxide thickness has been then reduced on following lots of approximately 30Å.

Due to the results obtained from the T84 routine, the electrical characterization has been performed at bench on the transistors considered representative of F6X target and corresponding to the trials with "coloured" background in the above Tables.

TRANSFER CHARACTERISTICS

Transfer characteristics have been measured at $V_d=100\text{mV}$, both with grounded substrate and biasing V_b up to 9V in order to take into account body effect. In Table 11 the subthreshold slope, ΔL and body effect coefficient γ have been reported for each type of transistor.

Table 11.

	L_{nom} (μm)	SS (mV/dec)	γ (V ^{1/2})	ΔL (μm)
n-ch HV nat	10/10	100.4	1.061	0.12
	10/0.8	101.8	0.919	
n-ch HV nat no-tub	10/10	85.8	0.854	0.14
	10/0.8	88.4	0.724	
n-ch LV LVS	10/10	92.9	0.885	0.05
	10/0.6	94.0	0.697	
n-ch LV nat	10/10	78.1	0.539	0.08
	10/1	78.7	0.439	
p-ch HV nat	10/10	88.4	0.684	0.05
	10/1	91.7	0.595	
p-ch LV LVS	10/10	79.8	0.399	0.05
	10/0.6	90.8	0.261	

DATA ANALYSIS

Transfer characteristics, output characteristics ($V_g=0, 1, 2...5V$ both for LV and HV) and breakdown curves (with grounded body, source and gate) of active transistors have been measured. Particular attention has been paid to minimum gate length. The data collected will be summarized for every kind of transistor.

1. *n-ch HV nat*

In Figs.1, 2, 3 transfer characteristics, output characteristics and breakdown curves of n-channel high voltage native transistors are respectively shown as function of gate length. Output curves only refer to the "short" ($W/L=10/0.8$) transistor. It can be observed from breakdown curves that transistors with gate length up to $0.7\mu m$ do not suffer from relevant punchthrough effect.

Fig.1

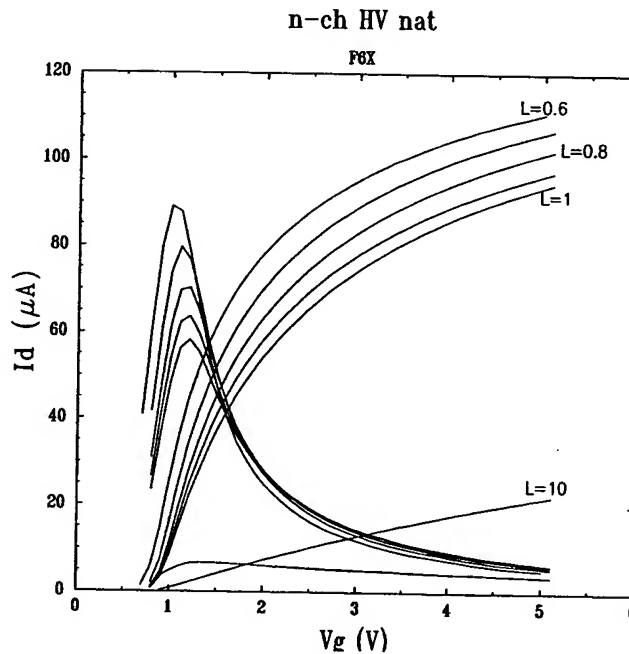


Fig.2

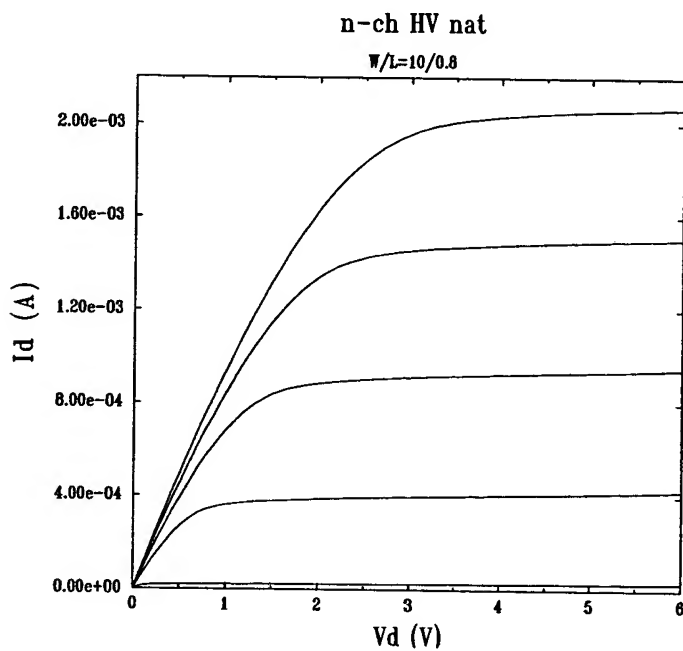
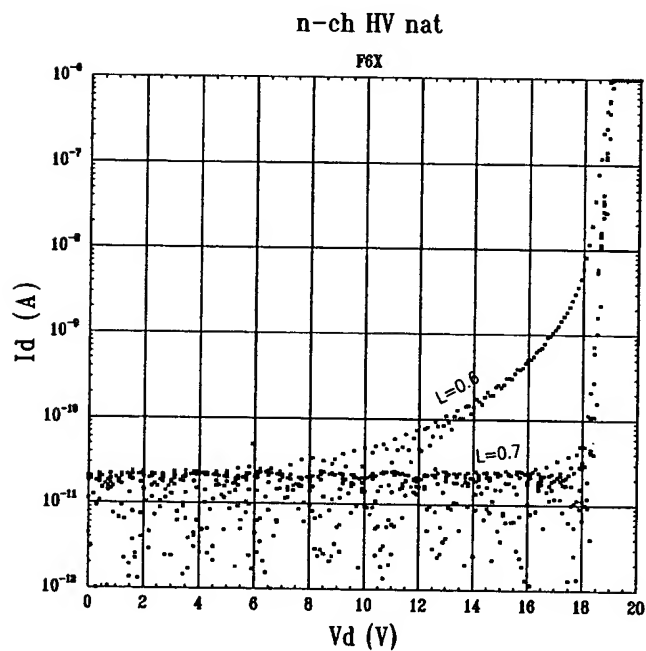


Fig.3



2. n-ch HV nat no-tub

In Figs.4, 5, 6 transfer characteristics, output characteristics and breakdown curves of n-channel high voltage native no-tub transistors are respectively shown. Output curves refer to the "short" ($W/L=10/0.8$) transistor. Due to the very low threshold voltage of this kind of transistor, a high level of subthreshold current is observed from breakdown curves. For this reason present data suggest that transistor gate length must be longer than $1\mu\text{m}$.

Fig.4

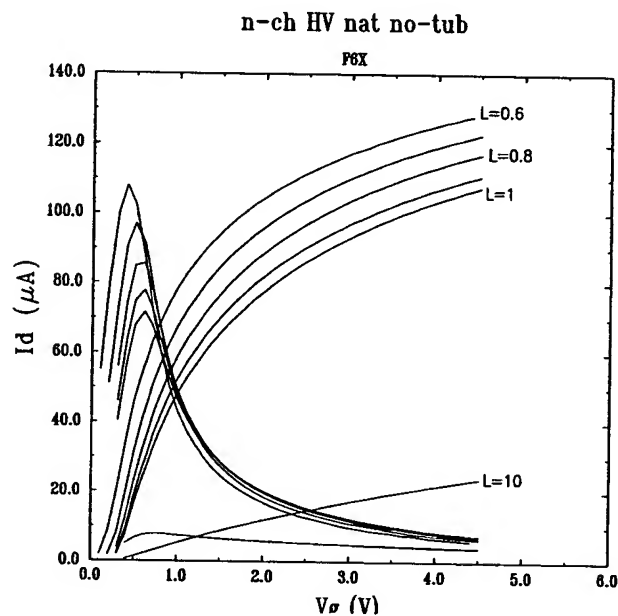


Fig.5

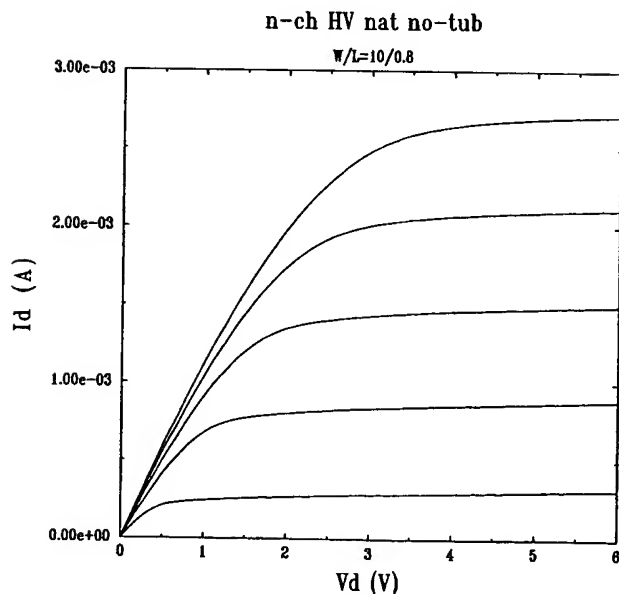
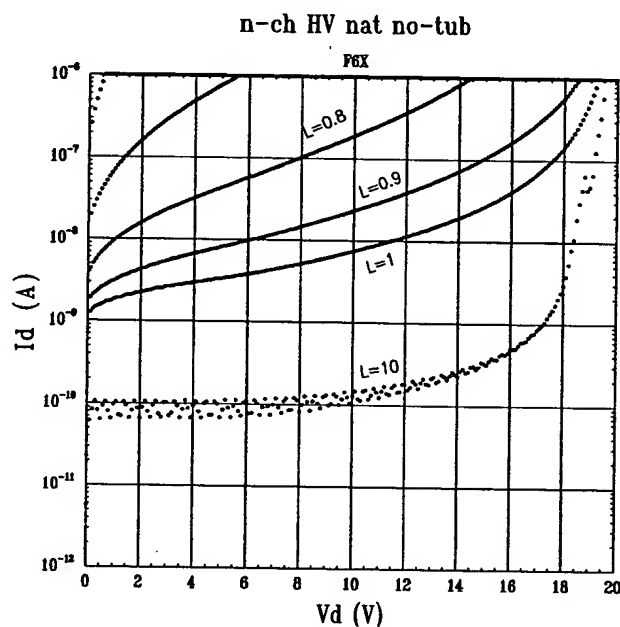
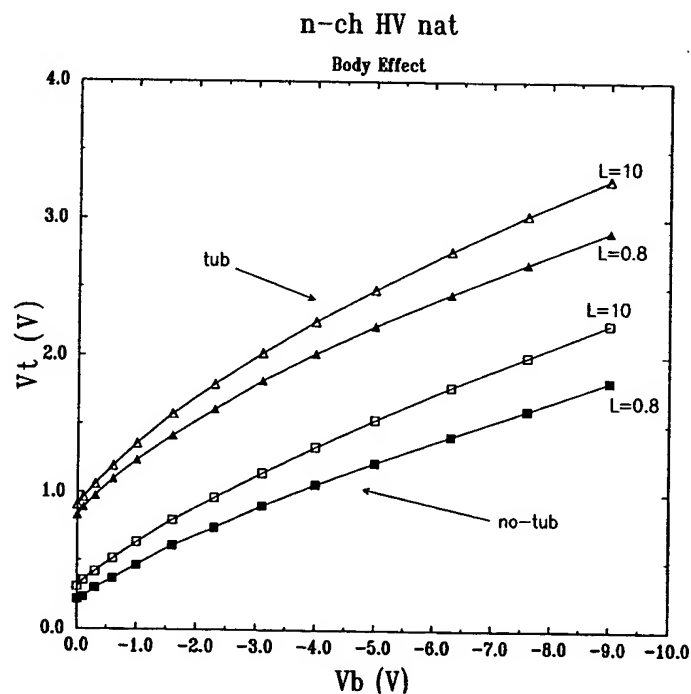


Fig.6



In Fig.7 the body effect curves are shown for square and short high voltage native transistors, both in the "tub" and "no-tub" options. As expected, the body effect on the threshold voltage is more marked for the "tub" ones .

Fig.7



3. n-ch LV LVS

In Figs.8, 9, 10 transfer characteristics, output characteristics and breakdown curves of n-channel low voltage enhanced transistors are respectively shown. Output curves refer to the "short" ($W/L=10/0.6$) transistor. In Fig.11 the effect of an increased dose of anti-punchthrough implant is shown (from $B\ 2.0 \times 10^{12}\text{ cm}^{-2}$ at 140 keV of Fig.10, to $B\ 4.0 \times 10^{12}\text{ cm}^{-2}$ at 140 keV of Fig.11). No substantial improvement is actually observed in the breakdown curves as function of gate length. It must be noted that a layout error has occurred in the Test Pattern which makes the 10/10 transistor a drain extension one. It can be identified from its higher breakdown voltage value.

Fig.8

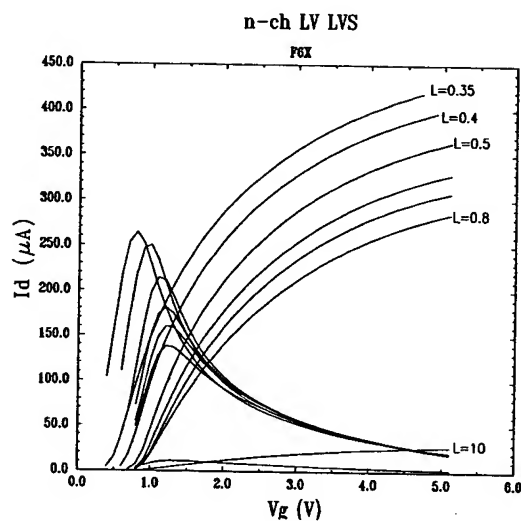


Fig.9

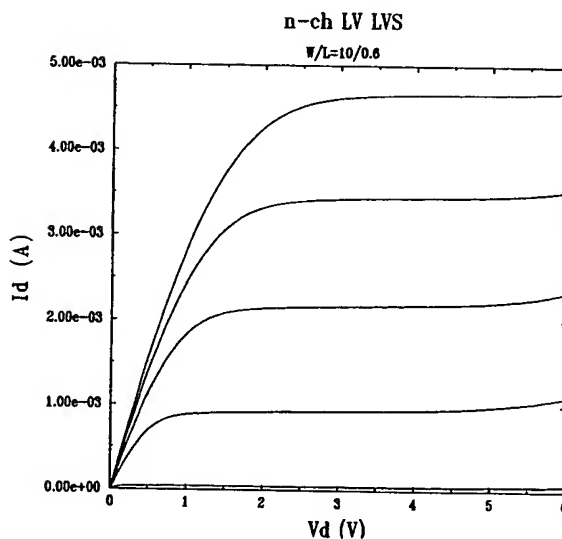


Fig.10 anti-PT implant: B 2.0e12 cm⁻² at 140 keV
n-ch LV LVS

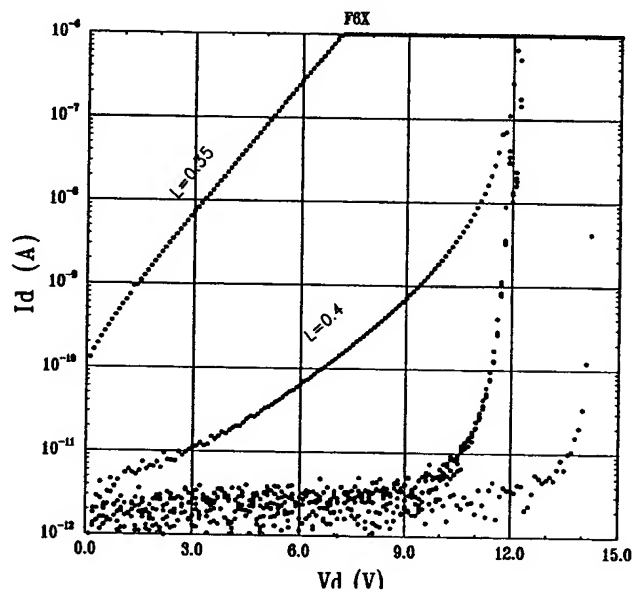
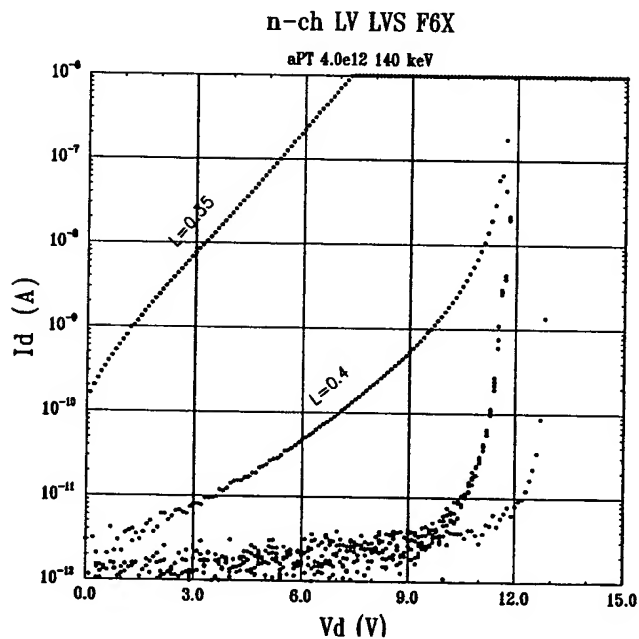


Fig.11 anti-PT implant: B 4.0e12 cm⁻² at 140 keV



4. n-ch LV nat

In Figs.12, 13, 14 transfer characteristics, output characteristics and breakdown curves of n-channel low voltage native transistors are respectively shown. Output curves refer to the "short" ($W/L=10/1$) transistor. Due to the low threshold voltage of this kind of transistor, a high level of subthreshold current is observed from breakdown curves. For this reason present data suggest that transistor gate length must be longer than $0.8\mu\text{m}$.

Fig.12

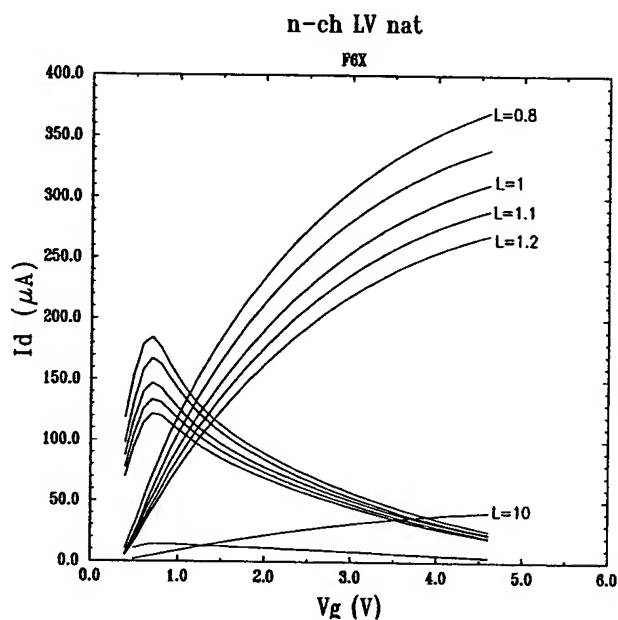


Fig.13

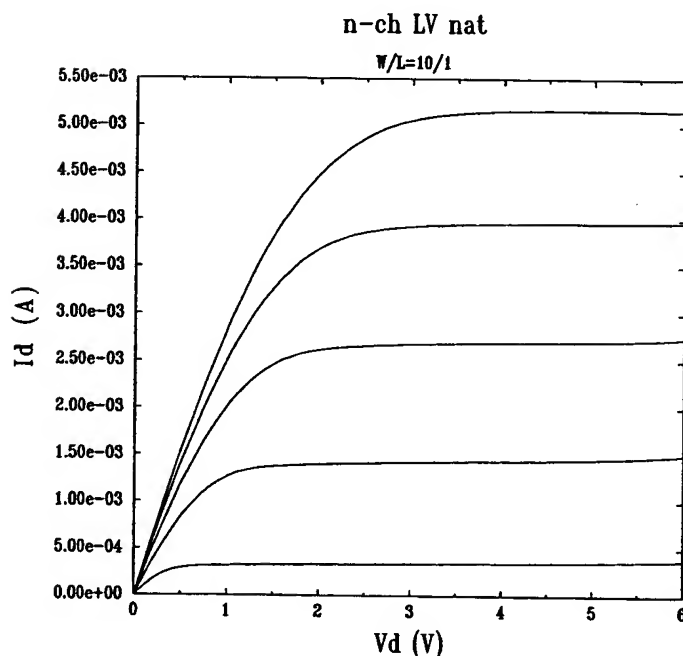
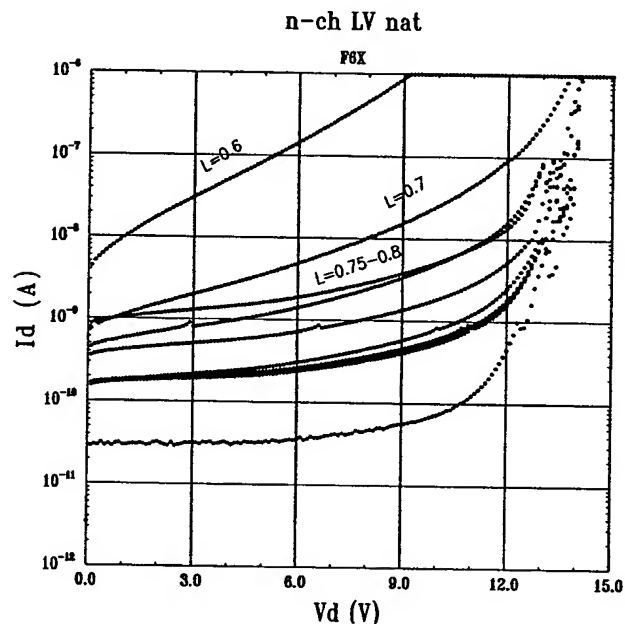
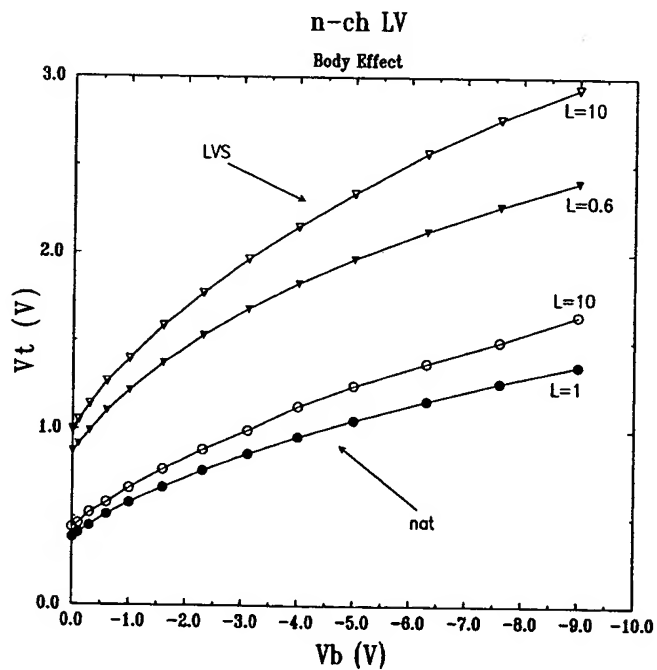


Fig.14



In Fig.15 the body effect curves are shown for square and short n-channel low voltage native and enhanced transistors.

Fig.15



5. p-ch HV nat

In Figs.16, 17, 18 transfer characteristics, output characteristics and breakdown curves of p-channel high voltage native transistors are respectively shown. Output curves refer to the "short" ($W/L=10/1$) transistor. An interesting result concerns the comparison between breakdown curves of this kind of transistor (Fig.18) and the p-ch HV "LVS" one (Fig.19). In both cases BV values higher than 18V are obtained with good performances as function of gate length.

Fig.16

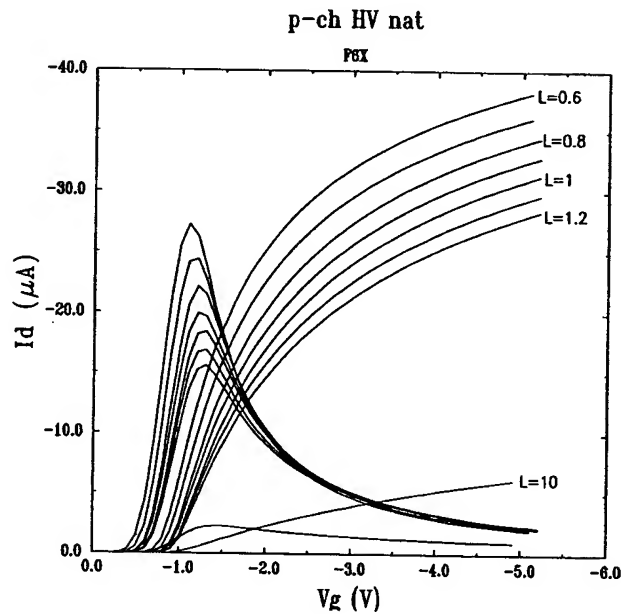


Fig.17

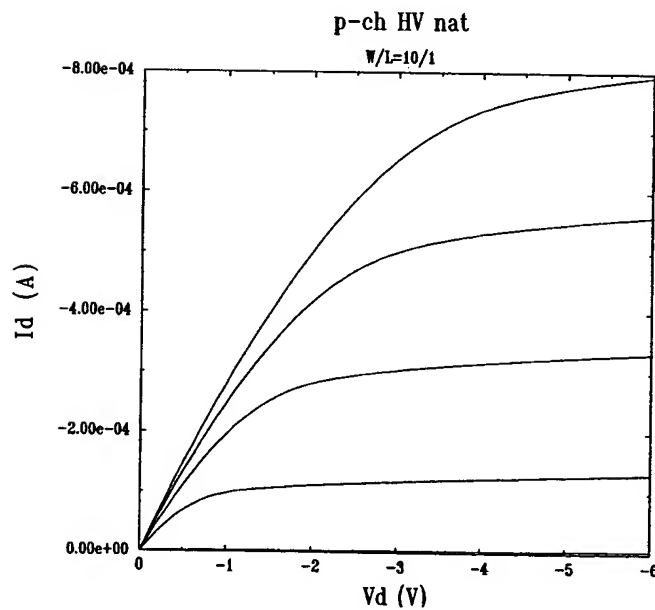


Fig.18

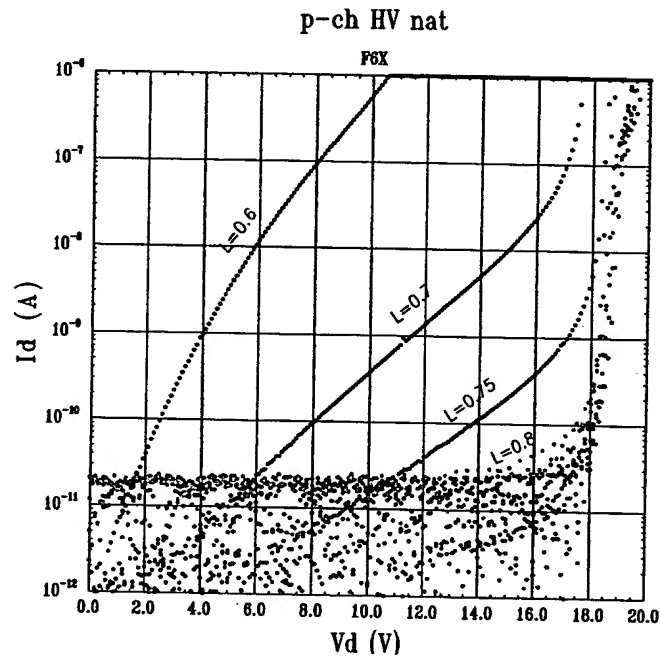
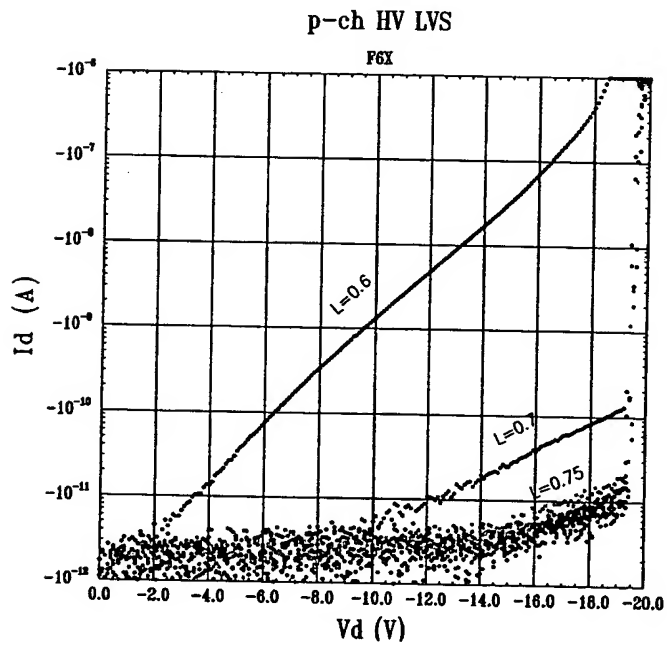
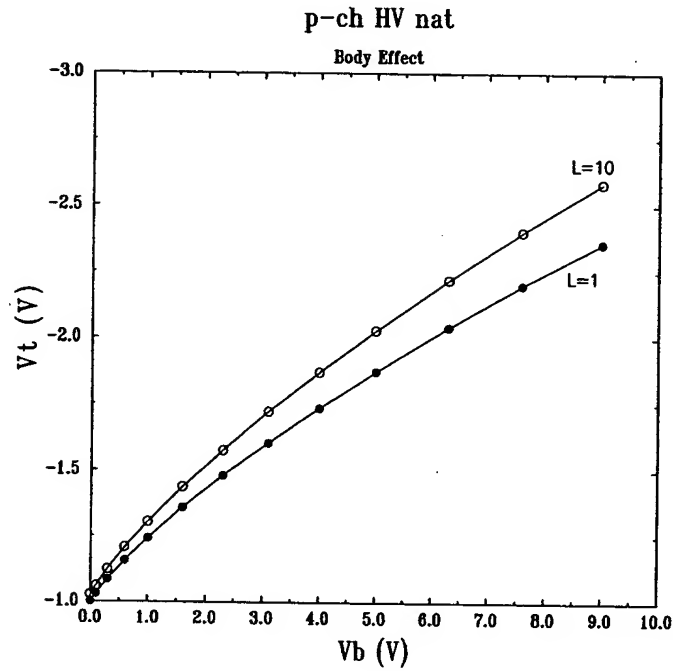


Fig.19



In Fig.20 the body effect curves are shown for square and short p-channel high voltage native transistors.

Fig.20



6. p-ch LV LVS

In Figs.21, 22, 23 transfer characteristics, output characteristics and breakdown curves of p-channel low voltage enhanced transistors are respectively shown. Output curves refer to the "short" ($W/L=10/0.6$) transistor. In Fig.24 the effect of an increased dose of p⁻ LDD implant is shown (from BF_2 $1.0 \times 10^{13} \text{ cm}^{-2}$ at 100 keV of Fig.23, to BF_2 $5.0 \times 10^{13} \text{ cm}^{-2}$ at 100 keV of Fig.24). It must be noted that the minimum gate length of this transistor appears marginal from breakdown curves, even with the lower p⁻ LDD implant dose (adopted as standard). This is a critical point which requires further work.

Fig.21

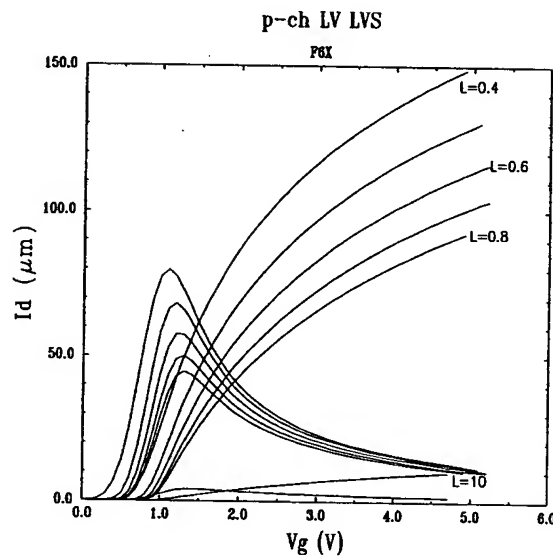


Fig.22

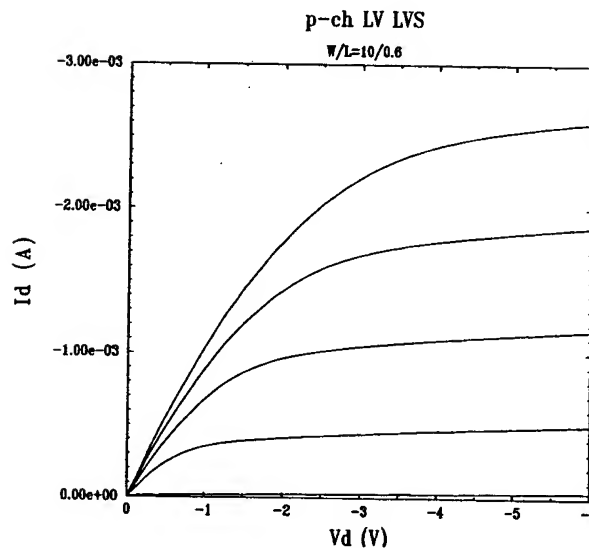


Fig.23 p⁻ LDD implant: BF₂ 1.0e13 cm⁻² at 100 keV

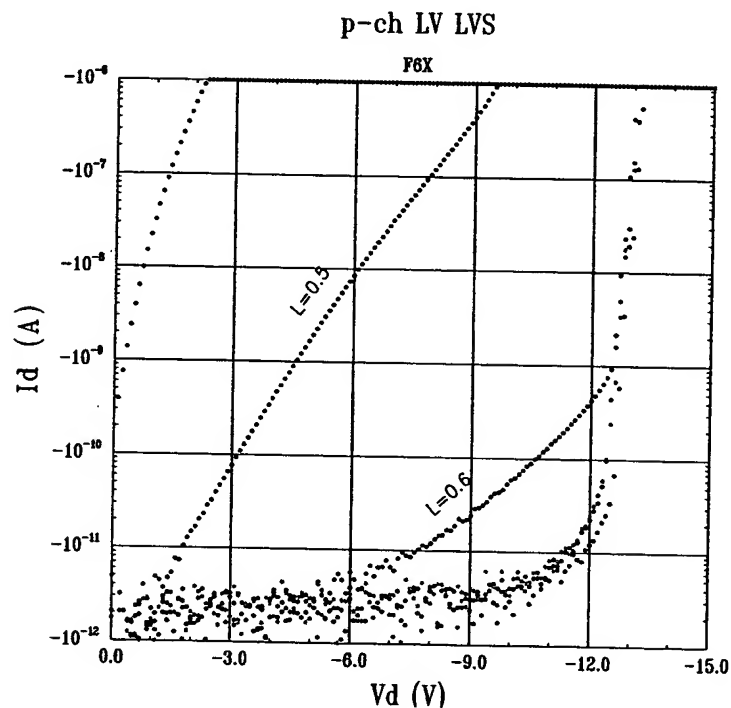
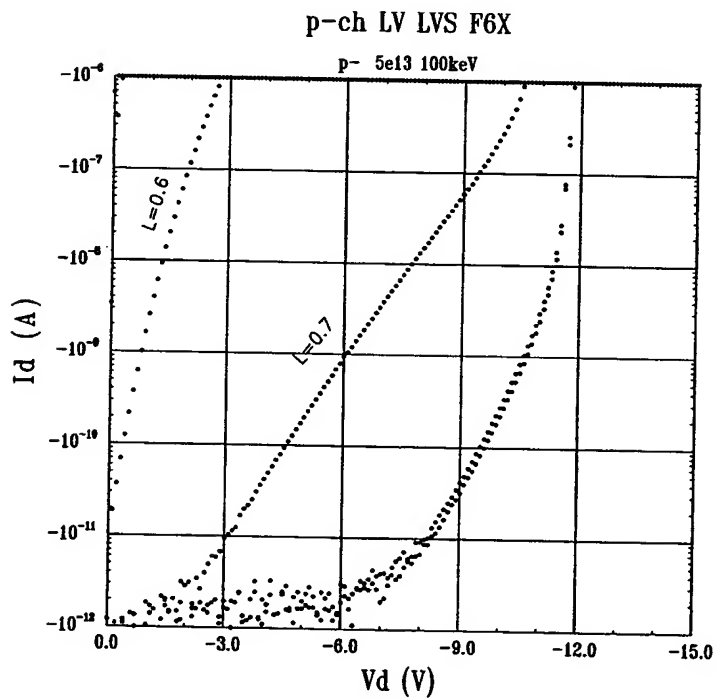
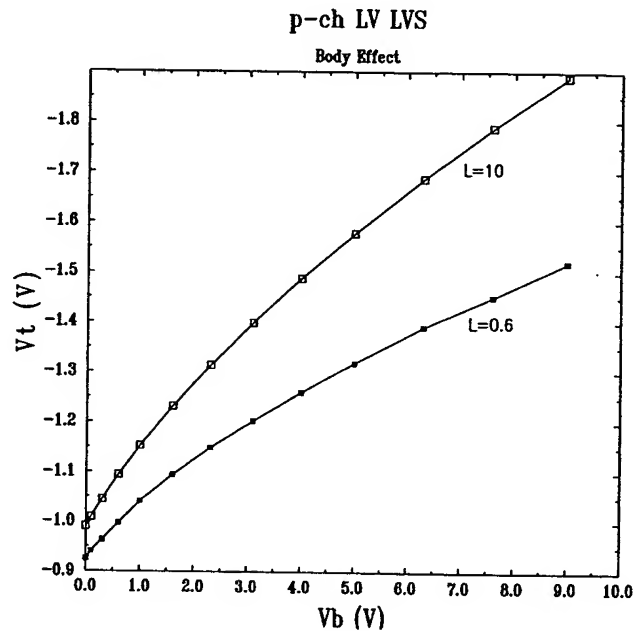


Fig.24 p⁻ LDD implant: BF₂ 5.0e13 cm⁻² at 100 keV



In Fig.25 the body effect curves are shown for square and short p-channel low voltage enhanced transistors.

Fig.25



CONCLUSIONS

A complete electrical characterization (at room temperature) of the active transistors available from F6X process flow has been performed. The results refer to the first lot out (SP process option), but they have been substantially confirmed by other two lots (T84 data). The electrical parameters target for F6X process have been almost obtained. Two critical points must now be addressed:

- ☐ electrical results must be confirmed by the Double-Poly process option
- ☐ gate length marginality of p-channel low voltage transistors has to be eliminated.

I hereby state that I am able to read and write in English and Italian and that the attached text is an accurate English translation of European Patent Application No. 98830694.0 filed on November 19, 1998.

A handwritten signature in black ink, appearing to be 'R. Iannucci', written over a horizontal line.

Robert Iannucci

TITLE: IMPROVED FIELD-EFFECT TRANSISTOR AND CORRESPONDING
MANUFACTURING METHOD

TECHNICAL FIELD

The present invention relates to an improved field effect transistor, and more
5 specifically to a field effect transistor having a variable doping profile.

More specifically, the invention relates to a field effect transistor integrated
on a semiconductor substrate with a relative active area comprising:

- a source region and a drain region formed in the semiconductor substrate,
- a channel region interposed between said source and drain regions and
10 having a predefined nominal width.

The invention also relates to a method of realizing a field effect transistor
integrated on a semiconductor substrate with a relative active area having a nominal width
comprising a source region and a drain region formed in said semiconductor substrate, a
channel region interposed between said source and drain regions and having a predefined
15 nominal width, the method comprising the steps of:

-selectively forming a oxide layer to define said relative active area on the
semiconductor substrate.

In particular but not exclusively, the invention relates to a field effect
transistor which operates at high voltages, this transistor being formed on a semiconductor
20 substrate and integrated with a well of N or P type and the description which follows is
made with reference to this field of application with the only objective of simplifying the
description.

PRIOR ART

As is well known, in the manufacturing of integrated circuit devices, in
25 particular EEPROM memories, that need high internal programming voltages, the need
comes up to integrate on the same chip transistors having low threshold voltage V_T and low
body factor.

A first known technical solution for manufacturing transistors with such
features is that of reducing the doping of the substrate or, in the well in which these devices

are formed. To this end "natural" transistors may be formed, that is without the use of additional doping implants on the semiconductor substrate where they are formed.

Although the technical problem is resolved, this first solution presents various drawbacks; in fact, in order to form these transistors with a low threshold voltage, it is necessary to introduce at least an additional mask in the standard process flows for the manufacture of the CMOS transistors. For instance, with the intention of masking the substrate portion where these transistors need to be formed.

Further on, to ensure the reliability of the parasitic field transistors that are formed between a portion of substrate in which these natural transistors are formed and a portion adjacent thereto, an insulating implant of P-iso (N-iso) type is usually formed on the entire active area, which requires a dedicated mask.

Associated with this kind of solution are further drawbacks such as:

- a large waste of area for guaranteeing a high enough threshold voltage of the parasitic transistor; and
- the threshold voltage of the "natural" transistors is determined by the doping of the substrate. In advanced processes substrates with low doping (or EPI substrates) are used which result in threshold voltages of the "depletion" active transistor;
- the introduction of an additional mask is necessary for performing an insulating implant P distinct from the P-well implant (or for differentiating the doping of the N-well implant in which the p-channel transistors are formed).

To modify the threshold voltage of such natural transistors (for example in order to obtain $V_T > 0$) two possibilities are given:

- an implant dedicated to the correction of the threshold voltage, that however needs a further dedicated mask with the increase of the costs of manufacturing;
- a blanket implant, that is without masking, to which, anyway, a reduction in the mobility of the complementary transistors (for example p-ch) is associated.

Further on, in some applications the use of more transistors is foreseen, with threshold voltages which differ of a small amount (for example $A V_T \cong 100 \text{ mV}$), which can be preferably defined according to the specific application (that is of the sub-circuit in which the transistor is inserted).

According to the prior art such result can be obtained through further implants for the adjustment of the threshold voltage of each transistor, each one requiring however a dedicated mask.

5 The technical problem on which the present invention is based is that of inventing a field effect transistor, having structural and functional characteristics that free the threshold voltage from the process parameters by intervening only on the structure layout in such a way to overcome the limitations and the drawbacks that still limit the transistors manufactured according to the prior art.

10 SUMMARY OF THE INVENTION

The solution idea on which the present invention is based is that of realizing a field effect transistor whose channel width is defined by a variable doping profile, which can be modified through changes in the layout of the structure. To obtain this variable doping profile, after the definition of the transistor active area, a mask is formed of greater width than the width of the active area; an external implant of doping is then carried out on
15 the transistor active area. Following the side diffusion of the doping due to thermal treatments, the doping profile of the width of the channel region of the transistor is modified and hence its threshold voltage.

Based on the solution idea, a field effect transistor of the type previously indicated is defined by the characterizing part of claim 1.

20 The problem is also resolved by a method of the type previously indicated which is defined by the characterizing part of claim 5

The features and the advantages of the transistor according to the invention will become clear from the following description, of an embodiment thereof, which is herein given as example for illustrative and not limiting purposes with reference to the
25 attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a layout view of a portion of a semiconductor substrate on which a field effect transistor according to the present invention is integrated.

Figure 2 is a cross-sectional diagram, along the line II of Figure 1, of the channel of the transistor according to the invention shown in Figure 1.

DETAILED DESCRIPTION

5 With reference to such Figures, a method is now disclosed for manufacturing field effect transistor 1 having a width of a channel region 5 defined by a variable doping profile.

10 The process steps and the structures described hereinbelow do not form a complete process flow for the manufacture of integrated circuits. The present invention can be put into practice together with the techniques for manufacturing integrated circuits used at the moment in the field, and only those commonly used process steps which are necessary for the comprehension of the present invention are included. Discussion of steps or processes well known to those skilled in the art has been abbreviated or eliminated for brevity.

15 The description which follows is reported with reference to a preferred example of embodiment with N-channel field effect transistors. For P-channel transistors, the types of conductivity that will be mentioned in the following shall be inverted.

20 The manufacturing of this type of transistors according to the present invention is particularly advantageous, when they are integrated onto a semiconductor substrate for example of P-type, and, in order to simplify the disclosure the following description relates to this particular field of application.

According to the invention, the MOS field effect transistor 1 is manufactured on a respective active area 8 of a predetermined nominal width W.

25 Such active area 8 comprises, in a known way, a portion of a semiconductor substrate 4 and is delimited by a layer 7 of insulating oxide. Inside the active area 8, a source region 2 and a drain region 3 are separated from one another by a portion of substrate 4 called channel region 5. The nominal width W of the channel region 5 is equal to the nominal length of the active area 8.

A floating gate region 13, formed by patterning a layer 12 of polysilicon is placed above the channel region 5 and is separated therefrom by means of a thin layer 11 of

gate oxide. A well 10, for example of P type, is formed underneath the insulating layer 7 of oxide and surrounds the active area 8 of the transistor 1.

In particular, the well 10 is implanted at a distance equal to $(W_M - W_N) / 2$ of the active area 8 in the direction of the width of the channel region 5, wherein W , is the width of a mask 9 used for realizing the implanted region 10.

As a consequence of the side diffusion of the dopant used for forming the well 10, doping is obtained for the effective width W_{eff} of the channel region 5 that varies with concentration starting from the edge of the well 10 (profile A in Figure 2) towards the center of the channel region (profiles B and C).

In this way, a parallel configuration is obtained of a series of transistors with infinitesimal differences in width W at an infinitesimally different threshold voltages, the concentration of which progressively decreases from the edge to the center of the channel.

The effective width W_{eff} of the channel region 5 is also function of the distance $(W_M - W_N)/2$ of the region 10 implanted by the active area 8.

According to the invention, as the effective width W_{eff} of the channel region 5 varies, and therefore as the distance from the active region 8 varies at which the well 10 is formed, so varies the doping profile of the width W_{eff} of the channel region 5 of the transistor, and therefore its threshold voltage V_T .

The process steps for manufacturing the transistors according to the invention are now described.

On the surface of a semiconductor substrate 4 of P-type, a thick layer 7 of oxide is selectively formed for defining an active area 8 on which the transistor 1 is formed.

As mentioned, such active area 8 has a nominal length that determines the nominal width of the channel region 5 of the transistor 1.

At this point, process steps are carried out in order to form the CMOS transistors in respective wells 10, for example of P-type, formed in the substrate 4. In a known way, a mask, for example of Pwell type, is formed on the semiconductor substrate 4, for example of P type.

According to the invention, this Pwell mask comprises a portion 9 of mask that covers the active area 8. This portion 9 has a width W_M at least greater than the width W_N of the active area 8.

Therefore an implant of P type is carried out in order to form the well 10 with a greater concentration than that of the substrate. Advantageously, thermal processes are carried out in order to let the implanted dopant of P type diffuse.

5 The profiles A, B and C of doping in Figure 2 illustrate the side diffusion of the dopant after the implantation and after the application of the thermal processes to the well 10.

As a consequence of the side diffusion of the dopant used for forming the well 10, the doping of the effective width W_{eff} of the channel region 5 is obtained that continuously varies from the edge of the well 10 towards the center of the channel region 5.

10 In particular, as the implanted region is of P type, the doping profile increases continuously from the center of the channel region 5 up to the edge of the active area 8.

Nothing prevents the implanted region 10 from being of N type; in such a case, the doping profile decreases with continuity from the center of the channel region 5 to the edge of the active area 5.

15 The distance between the two profiles A that delimit the width of the channel obviously depends on the width W_M of the mask 9.

As the width W_M of the mask 9 varies, so varies the doping profile as defined by the width W_{eff} of the channel region 5 and hence the threshold voltage V_T of the transistor 1 vary.

20 The process is completed by subsequent, conventional steps, which permit to realize: anti-punchthrough implants, implants for the correction of threshold voltage and all the further implants for the correction of threshold voltage; the formation of a layer 11 for defining gate oxides; the deposition of a layer of polysilicon 12 which is afterwards shaped for defining the gate regions 12; the implant of source region 2 and of drain 3 which are doped as N-type; intermediate dielectrics; lines of metallization; layers of passivation.

25 Speaking in broader terms, in order to modify the threshold voltage V_T of a transistor 1 manufactured according to an embodiment of the invention, it is sufficient to add to the known steps of the manufacturing steps of CMOS transistors, a mask of bigger dimension than the active area 8 of the transistor 1 as a function of the desired threshold

30

voltage V_T , in such a way to obtain the appropriate doping profile of the width of the channel.

Further on, by manufacturing the transistors 1 with the method according to the invention, it is possible to form in the same integrated circuit, transistors obtained with
5 the same sequence of implants and hence masks, but with a different doping profile for the channel and hence different threshold voltages V_T .

Advantageously, it is possible to obtain transistors 1 with different threshold voltage, even of a same first width W_1 , if a circuit solution is used that allows to connect in parallel two or more transistors with a second width W_2 smaller than the first width W_1 ;
10 once defined the end value for the width W_1 , such value can be divided in the parallel of a variable number of transistors, the side dimension W_2 of which determines the value of the final threshold voltage.

To sum up, by varying the value of the effective width W_{eff} of the transistor 1, its threshold voltage V_T is directly varied, without modifying the process steps for
15 manufacturing the CMOS transistors.

Further on, the effective width W_{eff} being equal, it is as well possible to obtain different values for the threshold voltage, by employing the parallel of more transistors 1.

CLAIMS

1. A field effect transistor integrated on a semiconductor substrate having an active area, the field effect transistor comprising:

a source region and a drain region formed in the semiconductor substrate;

5 a channel region interposed between said source and drain regions having a predefined nominal width, characterized in that the channel region has an effective width defined by a variable doping profile.

2. The field effect transistor according to claim 1, characterized in that the variable doping profile is one of a region implanted adjacent to the transistor.

10 3. The field effect transistor according to claim 2, characterized in that the effective width is a function of a distance of a region implanted by the active area.

4. The field effect transistor according to claim 1, characterized in that the doping profile has a minimum of concentration at a center of the channel region.

15 5. The field effect transistor according to claim 1, characterized in that the doping profile increases with continuity from a center of the channel region to an edge of the active area.

20 6. A method for manufacturing a field effect transistor integrated onto a semiconductor substrate with an active area having a nominal width the field effect transistor including a source region and a drain region formed in said semiconductor substrate, and a channel region interposed between said source and drain regions and having a nominal width, the method comprising the steps of:

forming said active area on the semiconductor substrate, characterized by comprising the steps of:

25 masking said active area with a mask of greater width than the nominal width of the active area;

implanting a dopant in the substrate around the mask in such a way that the channel region has an effective width defined by a variable doping profile.

7. The method for manufacturing a field effect transistor according to claim 6, characterized in that said dopant implant in the substrate around the mask forms a
5 region that determines said variable doping profile that defines the effective width of the channel region.

8. The method for manufacturing a field effect transistor according to claim 6 characterized in that said doping profile has a minimum of concentration at the center of the channel region.

ABSTRACT

5 A field effect transistor having a variable doping profile is presented. The field effect transistor is integrated on a semiconductor substrate with a respective active area of the substrate including a source and drain region. A channel region is interposed between the source and drain regions and has a predefined nominal width. The effective width of the channel region is defined by a variable doping profile.

10 (figure 2)